MITSUBISHI ELECTRIC

Programmable Controller

MELSEC Q series

QCPU User's Manual (Multiple CPU System)

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-Q26UD(E)HCPU
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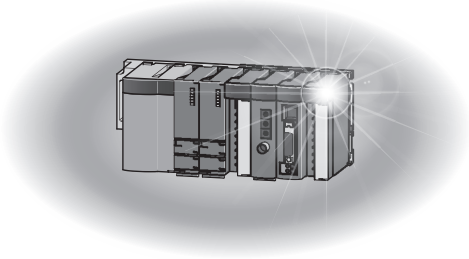


●SAFETY PRECAUTIONS●

(Read these precautions before using this product.)

Before using this product, please read this manual and the relevant manuals carefully and pay full attention to safety to handle the product correctly.

In this manual, the safety precautions are classified into two levels: "⚠WARNING" and "⚠CAUTION".

⚠WARNING	Indicates that incorrect handling may cause hazardous conditions, resulting in death or severe injury.
⚠CAUTION	Indicates that incorrect handling may cause hazardous conditions, resulting in minor or moderate injury or property damage.

Under some circumstances, failure to observe the precautions given under "⚠CAUTION" may lead to serious consequences.
Observe the precautions of both levels because they are important for personal and system safety.
Make sure that the end users read this manual and then keep the manual in a safe place for future reference.

[Design Precautions]

⚠ WARNING

● Configure safety circuits external to the programmable controller to ensure that the entire system operates safely even when a fault occurs in the external power supply or the programmable controller. Failure to do so may result in an accident due to an incorrect output or malfunction.

(1) Configure external safety circuits, such as an emergency stop circuit, protection circuit, and protective interlock circuit for forward/reverse operation or upper/lower limit positioning.

(2) The programmable controller stops its operation upon detection of the following status, and the output status of the system will be as shown below.

	Q series module	AnS/A series module
Overcurrent or overvoltage protection of the power supply module is activated.	All outputs are turned off	All outputs are turned off
The CPU module detects an error such as a watchdog timer error by the self-diagnostic function.	All outputs are held or turned off according to the parameter setting.	All outputs are turned off

All outputs may turn on when an error occurs in the part, such as I/O control part, where the programmable controller CPU cannot detect any error. To ensure safety operation in such a case, provide a safety mechanism or a fail-safe circuit external to the programmable controller. For a fail-safe circuit example, refer to the QCPU User's Manual (Hardware Design, Maintenance and Inspection).

(3) Outputs may remain on or off due to a failure of an output module relay or transistor. Configure an external circuit for monitoring output signals that could cause a serious accident.

[Design Precautions]

⚠ WARNING

- In an output module, when a load current exceeding the rated current or an overcurrent caused by a load short-circuit flows for a long time, it may cause smoke and fire. To prevent this, configure an external safety circuit, such as a fuse.
- Configure a circuit so that the programmable controller is turned on first and then the external power supply. If the external power supply is turned on first, an accident may occur due to an incorrect output or malfunction.
- For the operating status of each station after a communication failure, refer to manuals relevant to the network. Incorrect output or malfunction due to a communication failure may result in an accident.
- When connecting a peripheral with the CPU module or connecting an external device, such as a personal computer, with an intelligent function module to modify data of a running programmable controller, configure an interlock circuit in the program to ensure that the entire system will always operate safely. For other forms of control (such as program modification or operating status change) of a running programmable controller, read the relevant manuals carefully and ensure that the operation is safe before proceeding. Especially, when a remote programmable controller is controlled by an external device, immediate action cannot be taken if a problem occurs in the programmable controller due to a communication failure. To prevent this, configure an interlock circuit in the sequence program, and determine corrective actions to be taken between the external device and CPU module in case of a communication failure.

[Design Precautions]

⚠ CAUTION

- Do not install the control lines or communication cables together with the main circuit lines or power cables. Keep a distance of 100mm (3.94 inches) or more between them. Failure to do so may result in malfunction due to noise.
- When a device such as a lamp, heater, or solenoid valve is controlled through an output module, a large current (approximately ten times greater than normal) may flow when the output is turned from off to on. Take measures such as replacing the module with one having a sufficient current rating.
- After the CPU module is powered on or is reset, the time taken to enter the RUN status varies depending on the system configuration, parameter settings, and/or program size. Design circuits so that the entire system will always operate safely, regardless of the time.

[Installation Precautions]

⚠ CAUTION

- Use the programmable controller in an environment that meets the general specifications in the QCPU User's Manual (Hardware Design, Maintenance and Inspection). Failure to do so may result in electric shock, fire, malfunction, or damage to or deterioration of the product.
- To mount the module, while pressing the module mounting lever located in the lower part of the module, fully insert the module fixing projection(s) into the hole(s) in the base unit and press the module until it snaps into place. Incorrect mounting may cause malfunction, failure or drop of the module. When using the programmable controller in an environment of frequent vibrations, fix the module with a screw. Tighten the screw within the specified torque range. Undertightening can cause drop of the screw, short circuit, or malfunction. Overtightening can damage the screw and/or module, resulting in drop, short circuit, or malfunction.
- When using an extension cable, connect it to the extension cable connector of the base unit securely. Check the connection for looseness. Poor contact may cause incorrect input or output.
- When using a memory card, fully insert it into the memory card slot. Check that it is inserted completely. Poor contact may cause malfunction.
- When using an SD memory card, fully insert it into the SD memory card slot. Check that it is inserted completely. Poor contact may cause malfunction.
- Securely insert an extended SRAM cassette into the cassette connector of a CPU module. After insertion, close the cassette cover to prevent the cassette from coming off. Poor contact may cause malfunction.
- Shut off the external power supply (all phases) used in the system before mounting or removing the module. Failure to do so may result in damage to the product. A module can be replaced online (while power is on) on any MELSECNET/H remote I/O station or in the system where a CPU module supporting the online module change function is used. Note that there are restrictions on the modules that can be replaced online, and each module has its predetermined replacement procedure. For details, refer to the relevant sections in the QCPU User's Manual (Hardware Design, Maintenance and Inspection) and in the manual for the corresponding module.
- Do not directly touch any conductive parts and electronic components of the module, memory card, SD memory card, or extended SRAM cassette. Doing so can cause malfunction or failure of the module.
- When using a Motion CPU module and modules designed for motion control, check that the combinations of these modules are correct before applying power. The modules may be damaged if the combination is incorrect. For details, refer to the user's manual for the Motion CPU module.

[Wiring Precautions]

⚠ WARNING

- Shut off the external power supply (all phases) used in the system before wiring. Failure to do so may result in electric shock or damage to the product.
- After installation and wiring, attach the included terminal cover to the module before turning it on for operation. Failure to do so may result in electric shock.

[Wiring Precautions]

⚠ CAUTION

- Individually ground the FG and LG terminals of the programmable controller with a ground resistance of 100Ω or less. Failure to do so may result in electric shock or malfunction.
- Use applicable solderless terminals and tighten them within the specified torque range. If any spade solderless terminal is used, it may be disconnected when the terminal screw comes loose, resulting in failure.
- Check the rated voltage and terminal layout before wiring to the module, and connect the cables correctly. Connecting a power supply with a different voltage rating or incorrect wiring may cause a fire or failure.
- Connectors for external devices must be crimped or pressed with the tool specified by the manufacturer, or must be correctly soldered. Incomplete connections may cause short circuit, fire, or malfunction.
- Securely connect the connector to the module. Poor contact may cause malfunction.
- Do not install the control lines or communication cables together with the main circuit lines or power cables. Keep a distance of 100mm (3.94 inches) or more between them. Failure to do so may result in malfunction due to noise.
- Place the cables in a duct or clamp them. If not, dangling cable may swing or inadvertently be pulled, resulting in damage to the module or cables or malfunction due to poor connection.
- Check the interface type and correctly connect the cable. Incorrect wiring (connecting the cable to an incorrect interface) may cause failure of the module and external device.
- Tighten the terminal screws within the specified torque range. Undertightening can cause short circuit, fire, or malfunction. Overtightening can damage the screw and/or module, resulting in drop, short circuit, or malfunction.
- Prevent foreign matter such as dust or wire chips from entering the module. Such foreign matter can cause a fire, failure, or malfunction.
- A protective film is attached to the top of the module to prevent foreign matter, such as wire chips, from entering the module during wiring. Do not remove the film during wiring. Remove it for heat dissipation before system operation.
- When disconnecting the cable from the module, do not pull the cable by the cable part. For the cable with connector, hold the connector part of the cable. For the cable connected to the terminal block, loosen the terminal screw. Pulling the cable connected to the module may result in malfunction or damage to the module or cable.
- Mitsubishi programmable controllers must be installed in control panels. Connect the main power supply to the power supply module in the control panel through a relay terminal block. Wiring and replacement of a power supply module must be performed by qualified maintenance personnel with knowledge of protection against electric shock. For wiring methods, refer to the QCPU User's Manual (Hardware Design, Maintenance and Inspection).

[Startup and Maintenance Precautions]

⚠ WARNING

- Do not touch any terminal while power is on. Doing so will cause electric shock or malfunction.
- Correctly connect the battery connector. Do not charge, disassemble, heat, short-circuit, solder, or throw the battery into the fire. Also, do not expose it to liquid or strong shock. Doing so will cause the battery to produce heat, explode, ignite, or leak, resulting in injury and fire.
- Shut off the external power supply (all phases) used in the system before cleaning the module or retightening the terminal screws, connector screws, or module fixing screws. Failure to do so may result in electric shock or cause the module to fail or malfunction.

[Startup and Maintenance Precautions]

⚠ CAUTION

- Before performing online operations (especially, program modification, forced output, and operating status change) for the running CPU module from the peripheral device connected, read relevant manuals carefully and ensure the safety. Improper operation may damage machines or cause accidents.
- Do not disassemble or modify the modules. Doing so may cause failure, malfunction, injury, or a fire.
- Use any radio communication device such as a cellular phone or PHS (Personal Handy-phone System) more than 25cm (9.85 inches) away in all directions from the programmable controller. Failure to do so may cause malfunction.
- Shut off the external power supply (all phases) used in the system before mounting or removing the module. Failure to do so may cause the module to fail or malfunction. A module can be replaced online (while power is on) on any MELSECNET/H remote I/O station or in the system where a CPU module supporting the online module change function is used. Note that there are restrictions on the modules that can be replaced online, and each module has its predetermined replacement procedure. For details, refer to the relevant sections in the QCPU User's Manual (Hardware Design, Maintenance and Inspection) and in the manual for the corresponding module.
- After the first use of the product, do not perform each of the following operations more than 50 times (IEC 61131-2/JIS B 3502 compliant).
  Exceeding the limit may cause malfunction.
  - Mounting/removing the module to/from the base unit
  - Inserting/removing the extended SRAM cassette to/from the CPU module
  - Mounting/removing the terminal block to/from the module
- After the first use of the product, do not insert/remove the SD memory card to/from the CPU module more than 500 times. Exceeding the limit may cause malfunction.
- Do not drop or apply shock to the battery to be installed in the module. Doing so may damage the battery, causing the battery fluid to leak inside the battery. If the battery is dropped or any shock is applied to it, dispose of it without using.
- Before handling the module, touch a grounded metal object to discharge the static electricity from the human body. Failure to do so may cause the module to fail or malfunction.

[Disposal Precautions]

⚠ CAUTION
● When disposing of this product, treat it as industrial waste. When disposing of batteries, separate them from other wastes according to the local regulations. (For the Battery Directive in EU member states, refer to the QCPU User's Manual (Hardware Design, Maintenance and Inspection).)

[Transportation Precautions]

⚠ CAUTION
● When transporting lithium batteries, follow the transportation regulations. (For details of the regulated models, refer to the QCPU User's Manual (Hardware Design, Maintenance and Inspection).)

●CONDITIONS OF USE FOR THE PRODUCT●

(1) Mitsubishi programmable controller ("the PRODUCT") shall be used in conditions;
i) where any problem, fault or failure occurring in the PRODUCT, if any, shall not lead to any major or serious accident; and
ii) where the backup and fail-safe function are systematically or automatically provided outside of the PRODUCT for the case of any problem, fault or failure occurring in the PRODUCT.

(2) The PRODUCT has been designed and manufactured for the purpose of being used in general industries.
MITSUBISHI SHALL HAVE NO RESPONSIBILITY OR LIABILITY (INCLUDING, BUT NOT LIMITED TO ANY AND ALL RESPONSIBILITY OR LIABILITY BASED ON CONTRACT, WARRANTY, TORT, PRODUCT LIABILITY) FOR ANY INJURY OR DEATH TO PERSONS OR LOSS OR DAMAGE TO PROPERTY CAUSED BY the PRODUCT THAT ARE OPERATED OR USED IN APPLICATION NOT INTENDED OR EXCLUDED BY INSTRUCTIONS, PRECAUTIONS, OR WARNING CONTAINED IN MITSUBISHI'S USER, INSTRUCTION AND/OR SAFETY MANUALS, TECHNICAL BULLETINS AND GUIDELINES FOR the PRODUCT.
("Prohibited Application")
Prohibited Applications include, but not limited to, the use of the PRODUCT in;

- Nuclear Power Plants and any other power plants operated by Power companies, and/or any other cases in which the public could be affected if any problem or fault occurs in the PRODUCT.
- Railway companies or Public service purposes, and/or any other cases in which establishment of a special quality assurance system is required by the Purchaser or End User.
- Aircraft or Aerospace, Medical applications, Train equipment, transport equipment such as Elevator and Escalator, Incineration and Fuel devices, Vehicles, Manned transportation, Equipment for Recreation and Amusement, and Safety devices, handling of Nuclear or Hazardous Materials or Chemicals, Mining and Drilling, and/or other applications where there is a significant risk of injury to the public or property.

Notwithstanding the above restrictions, Mitsubishi may in its sole discretion, authorize use of the PRODUCT in one or more of the Prohibited Applications, provided that the usage of the PRODUCT is limited only for the specific applications agreed to by Mitsubishi and provided further that no special quality assurance or fail-safe, redundant or other safety features which exceed the general specifications of the PRODUCTs are required. For details, please contact the Mitsubishi representative in your region.

INTRODUCTION

This manual describes the system configurations, functions, and communication methods with external devices required in a multiple CPU system.

Before using this product, please read this manual and the relevant manuals carefully and develop familiarity with the functions and performance of the Q series programmable controller to handle the product correctly.
When applying the program examples introduced in this manual to the actual system, ensure the applicability and confirm that it will not cause system control problems.

■Relevant CPU modules:

CPU module	Model
Basic model QCPU	Q00CPU, Q01CPU
High Performance model QCPU	Q02(H)CPU, Q06HCPU, Q12HCPU, Q25HCPU
Process CPU	Q02PHCPU, Q06PHCPU, Q12PHCPU, Q25PHCPU
Universal model QCPU	Q00UCPU, Q01UCPU, Q02UCPU, Q03UD(E)CPU, Q03UDVCPU, Q04UD(E)HCPU, Q04UDVCPU, Q04UDPVCPU, Q06UD(E)HCPU, Q06UDVCPU, Q06UDPVCPU, Q10UD(E)HCPU, Q13UD(E)HCPU, Q13UDVCPU, Q13UDPVCPU, Q20UD(E)HCPU, Q26UD(E)HCPU, Q26UDVCPU, Q26UDPVCPU, Q50UDEHCPU, Q100UDEHCPU

Remark

- This manual does not describe the specifications and precautions of the power supply modules, base units, extension cables, memory cards, SD memory cards, extended SRAM cassettes, and batteries as well as the peripheral configurations.
  QCPU User's Manual (Hardware Design, Maintenance and Inspection)
- For the functions of CPU modules when used in a system other than a multiple CPU system, refer to the following.
  User's Manual (Function Explanation, Program Fundamentals) for the CPU module used

Memo

CONTENTS

MANUALS

To understand the main specifications, functions, and usage of the CPU module, refer to the basic manuals. Read other manuals as well when using a different type of CPU module and its functions. Order each manual as needed, referring to the following lists.

The numbers in the "CPU module" and the respective modules are as follows.

Number	CPU module	Number	CPU module
1)	Basic model QCPU	3)	Process CPU
2)	High Performance model QCPU	4)	Universal model QCPU

●: Basic manual, ○ : Other CPU module manuals/Use them to utilize functions.

(1) CPU module user's manual

Manual name <manual number (model code)>	Description	CPU module			
		1)	2)	3)	4)
QCPU User's Manual (Hardware Design, Maintenance and Inspection) <SH-080483ENG (13JR73)>	Specifications of the hardware (CPU modules, power supply modules, base units, extension cables, memory cards, SD memory cards, and extended SRAM cassettes), system maintenance and inspection, troubleshooting, and error codes	●	●	●	●
QnUCPU User's Manual (Function Explanation, Program Fundamentals) <SH-080807ENG (13JZ27)>	Functions, methods, and devices for programming				●
Qn(H)/QnPH/QnPRHCPU User's Manual (Function Explanation, Program Fundamentals) <SH-080808ENG (13JZ28)>	Functions, methods, and devices for programming	●	●	●	
QnUCPU User's Manual (Communication via Built-in Ethernet Port) <SH-080811ENG (13JZ29)>	Detailed description of communication via the built-in Ethernet ports of the CPU module				○
QnUDVCPU/LCPU User's Manual (Data Logging Function) <SH-080893ENG (13JZ39)>	Detailed description of the data logging function of the CPU module				○

(2) Programming manual

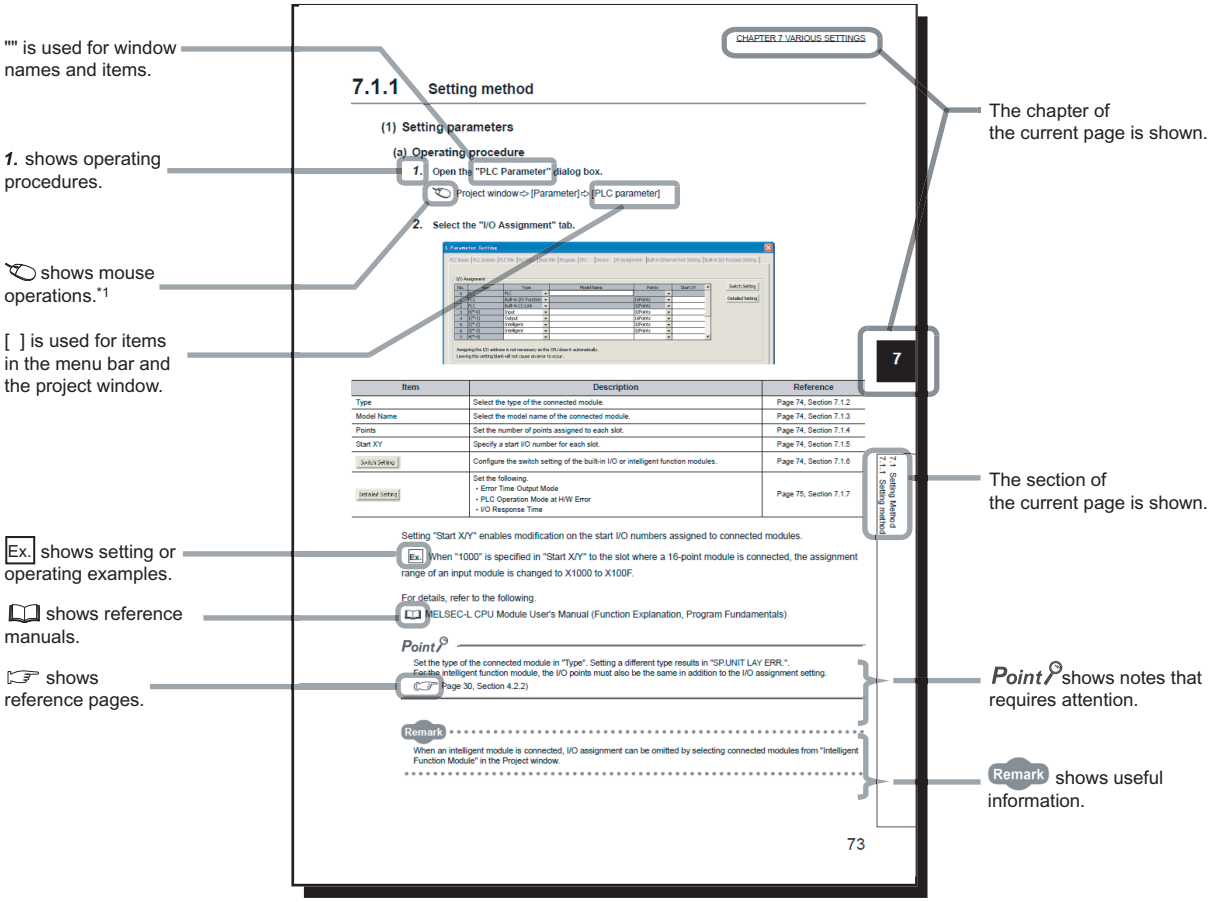
Manual name <manual number (model code)>	Description	CPU module			
		1)	2)	3)	4)
MELSEC-Q/L Programming Manual (Common Instruction) <SH-080809ENG (13JW10)>	Detailed description and usage of instructions used in programs	●	●	●	●
MELSEC-Q/L/QnA Programming Manual (SFC) <SH-080041 (13JF60)>	System configuration, specifications, functions, programming, and error codes for SFC (MELSAP3) programs	○	○	○	○
MELSEC-Q/L Programming Manual (MELSAP-L) <SH-080076 (13JF61)>	System configuration, specifications, functions, programming, and error codes for SFC (MELSAP-L) programs	○	○	○	○
MELSEC-Q/L Programming Manual (Structured Text) <SH-080366E (13JF68)>	System configuration and programming using structured text language	○	○	○	○
MELSEC-Q/L/QnA Programming Manual (PID Control Instructions) <SH-080040 (13JF59)>	Dedicated instructions for PID control	○	○		○
MELSEC-Q Programming/Structured Programming Manual (Process Control Instructions) <SH-080316E (13JF67)>	Dedicated instructions for process control			○	

(3) Operating manual

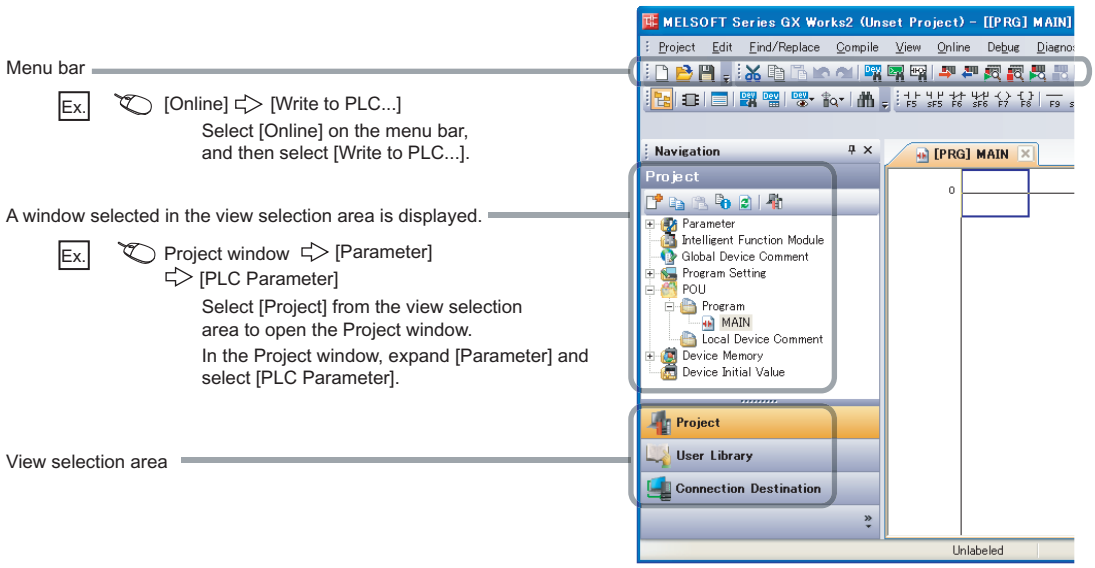
Manual name <manual number (model code)>	Description	CPU module			
		1)	2)	3)	4)
GX Works2 Version 1 Operating Manual (Common) <SH-080779ENG (13JU63)>	System configuration, parameter settings, and online operations (common to Simple project and Structured project) of GX Works2	●	●	●	●
GX Developer Version 8 Operating Manual <SH-080373E (13JU41)>	Operating methods of GX Developer, such as programming, printing, monitoring, and debugging	○	○	○	○

MANUAL PAGE ORGANIZATION

In this manual, pages are organized and the symbols are used as shown below.
The following page illustration is for explanation purpose only, and is different from the actual pages.



*1 The mouse operation example is provided below. (For GX Works2)



TERMS

Unless otherwise specified, this manual uses the following generic terms and abbreviations.

* □ indicates a part of the model or version.

Ex. Q33B, Q35B, Q38B, Q312B→Q3□B

Term	Description
■ Series	
Q series	An abbreviation for the Mitsubishi Electric MELSEC-Q series programmable controller
AnS series	An abbreviation for compact types of the Mitsubishi Electric MELSEC-A series programmable controller
A series	An abbreviation for large types of the Mitsubishi Electric MELSEC-A series programmable controller
■ CPU module type	
CPU module	A generic term for the Basic model QCPU, High Performance model QCPU, Process CPU, Universal model QCPU, Motion CPU, C Controller module, and PC CPU module. The term in this manual does not include the Redundant CPU because it cannot be used in a multiple CPU system.
QCPU	A generic term for the Basic model QCPU, High Performance model QCPU, Process CPU, and Universal model QCPU. The term in this manual does not include the Redundant CPU because it cannot be used in a multiple CPU system.
Basic model QCPU	A generic term for the Q00CPU and Q01CPU. The term in this manual does not include the Q00JCPU because it cannot be used in a multiple CPU system.
High Performance model QCPU	A generic term for the Q02CPU, Q02HCPU, Q06HCPU, Q12HCPU, and Q25HCPU
Process CPU	A generic term for the Q02PHCPU, Q06PHCPU, Q12PHCPU, and Q25PHCPU
Universal model QCPU	A generic term for the Q00UCPU, Q01UCPU, Q02UCPU, Q03UDCPU, Q03UDVCPU, Q03UDECPU, Q04UDHCPU, Q04UDVCPU, Q04UDPVCPU, Q04UDEHCPU, Q06UDHCPU, Q06UDVCPU, Q06UDPVCPU, Q06UDEHCPU, Q10UDHCPU, Q10UDEHCPU, Q13UDHCPU, Q13UDVCPU, Q13UDPVCPU, Q13UDEHCPU, Q20UDHCPU, Q20UDEHCPU, Q26UDHCPU, Q26UDVCPU, Q26UDPVCPU, Q26UDEHCPU, Q50UDEHCPU, and Q100UDEHCPU. The term in this manual does not include the Q00UJCPU because it cannot be used in a multiple CPU system.
Built-in Ethernet port QCPU	A generic term for the Q03UDVCPU, Q03UDECPU, Q04UDVCPU, Q04UDPVCPU, Q04UDEHCPU, Q06UDVCPU, Q06UDPVCPU, Q06UDEHCPU, Q10UDEHCPU, Q13UDVCPU, Q13UDPVCPU, Q13UDEHCPU, Q20UDEHCPU, Q26UDVCPU, Q26UDPVCPU, Q26UDEHCPU, Q50UDEHCPU, and Q100UDEHCPU
High-speed Universal model QCPU	A generic term for the Q03UDVCPU, Q04UDVCPU, Q06UDVCPU, Q13UDVCPU, and Q26UDVCPU
Universal model Process CPU	A generic term for the Q04UDPVCPU, Q06UDPVCPU, Q13UDPVCPU, and Q26UDPVCPU
Motion CPU	A generic term for the Mitsubishi Electric motion controllers: Q172CPUN, Q173CPUN, Q172HCPU, Q173HCPU, Q172CPUN-T, Q173CPUN-T, Q172HCPU-T, Q173HCPU-T, Q172DCPU, Q173DCPU, Q172DCPU-S1, Q173DCPU-S1, Q172DSCPU, and Q173DSCPU
PC CPU module	A generic term for the MELSEC-Q series-compatible PC CPU modules manufactured by CONTEC Co., Ltd: PPC-CPU686(MS)-64, PPC-CPU686(MS)-128, and PPC-CPU852(MS)-512
C Controller module	A generic term for the C Controller modules: Q06CCPU-V, Q06CCPU-V-B, Q12DCCPU-V, Q24DHCCPU-V, Q24DHCCPU-VG, Q24DHCCPU-LS, and Q26DHCCPU-LS.

Term	Description
■ CPU module model	
Qn(H)CPU	A generic term for the Q02CPU, Q02HCPU, Q06HCPU, Q12HCPU, and Q25HCPU
QnPHCPU	A generic term for the Q02PHCPU, Q06PHCPU, Q12PHCPU, and Q25PHCPU
QnUCPU	A generic term for the Q00UCPU, Q01UCPU, Q02UCPU, Q03UDCPU, Q03UDVCPU, Q03UDECPU, Q04UDHCPU, Q04UDVCPU, Q04UDPVCPU, Q04UDEHCPU, Q06UDHCPU, Q06UDVCPU, Q06UDPVCPU, Q06UDEHCPU, Q10UDHCPU, Q10UDEHCPU, Q13UDHCPU, Q13UDVCPU, Q13UDPVCPU, Q13UDEHCPU, Q20UDHCPU, Q20UDEHCPU, Q26UDHCPU, Q26UDVCPU, Q26UDPVCPU, Q26UDEHCPU, Q50UDEHCPU, and Q100UDEHCPU. The term in this manual does not include the Q00UJCPU because it cannot be used in a multiple CPU system.
QnU(D)(H)CPU	A generic term for the Q00UCPU, Q01UCPU, Q02UCPU, Q03UDCPU, Q04UDHCPU, Q06UDHCPU, Q10UDHCPU, Q13UDHCPU, Q20UDHCPU, and Q26UDHCPU. The term in this manual does not include the Q00UJCPU because it cannot be used in a multiple CPU system.
QnUDVCPU	A generic term for the Q03UDVCPU, Q04UDVCPU, Q06UDVCPU, Q13UDVCPU, and Q26UDVCPU
QnUDPVCPU	A generic term for the Q04UDPVCPU, Q06UDPVCPU, Q13UDPVCPU, and Q26UDPVCPU
QnUDE(H)CPU	A generic term for the Q03UDECPU, Q04UDEHCPU, Q06UDEHCPU, Q10UDEHCPU, Q13UDEHCPU, Q20UDEHCPU, Q26UDEHCPU, Q50UDEHCPU, and Q100UDEHCPU
Q172CPUN(-T)	A generic term for the Q172CPUN and Q172CPUN-T
Q173CPUN(-T)	A generic term for the Q173CPUN and Q173CPUN-T
Q172HCPU(-T)	A generic term for the Q172HCPU and Q172HCPU-T
Q173HCPU(-T)	A generic term for the Q173HCPU and Q173HCPU-T
Q172DCPU(-S1)	A generic term for the Q172DCPU and Q172DCPU-S1
Q173DCPU(-S1)	A generic term for the Q173DCPU and Q173DCPU-S1
■ Base unit type	
Base unit	A generic term for the main base unit, extension base unit, slim type main base unit, redundant power main base unit, redundant power extension base unit, and multiple CPU high speed main base unit. The term in this manual does not include the redundant type extension base unit because it cannot be used in a multiple CPU system.
Main base unit	A generic term for the Q3□B, Q3□SB, Q3□RB, and Q3□DB
Extension base unit	A generic term for the Q5□B, Q6□B, Q6□RB, QA1S5□B, QA1S6□B, QA1S6ADP+A1S5□B/A1S6□B, QA6□B, and QA6ADP+A5□B/A6□B. The term in this manual does not include the Q6□WRB because it cannot be used in a multiple CPU system.
Slim type main base unit	Another term for the Q3□SB
Redundant power main base unit	Another term for the Q3□RB
Redundant power extension base unit	Another term for the Q6□RB
Multiple CPU high speed main base unit	Another term for the Q3□DB
Redundant power supply base unit	A generic term for the redundant power main base unit and redundant power extension base unit
■ Base unit model	
Q3□B	A generic term for the Q33B, Q35B, Q38B, and Q312B main base units
Q3□SB	A generic term for the Q32SB, Q33SB, and Q35SB slim type main base units
Q3□RB	Another term for the Q38RB redundant power main base unit
Q3□DB	A generic term for the Q35DB, Q38DB, and Q312DB multiple CPU high speed main base units
Q5□B	A generic term for the Q52B and Q55B extension base units

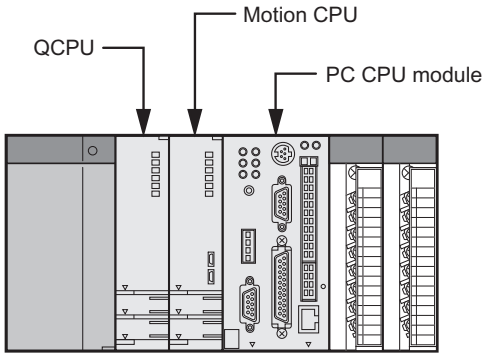
Term	Description
Q6□B	A generic term for the Q63B, Q65B, Q68B, and Q612B extension base units
Q6□RB	Another term for the Q68RB redundant power extension base unit
QA1S5□B	Another term for the QA1S51B extension base unit
QA1S6□B	A generic term for the QA1S65B and QA1S68B extension base units
QA6□B	A generic term for the QA65B and QA68B extension base units
A5□B	A generic term for the A52B, A55B, and A58B extension base units
A6□B	A generic term for the A62B, A65B, and A68B extension base units
QA6ADP+A5□B/A6□B	An abbreviation for a large type extension base unit where the QA6ADP is mounted
QA1S6ADP+A1S5□B/A1S6□B	An abbreviation for a small type extension base unit where the QA1S6ADP is mounted
■ Power supply module	
Power supply module	A generic term for the Q series power supply module, AnS series power supply module, A series power supply module, slim type power supply module, and redundant power supply module
Q series power supply module	A generic term for the Q61P-A1, Q61P-A2, Q61P, Q61P-D, Q62P, Q63P, Q64P, and Q64PN power supply modules
AnS series power supply module	A generic term for the A1S61PN, A1S62PN, and A1S63P power supply modules
A series power supply module	A generic term for the A61P, A61PN, A62P, A63P, A68P, A61PEU, and A62PEU power supply modules
Slim type power supply module	An abbreviation for the Q61SP slim type power supply module
Redundant power supply module	A generic term for the Q63RP and Q64RP redundant power supply modules
Life detection power supply module	An abbreviation for the Q61P-D life detection power supply module
■ Network module	
CC-Link IE module	A generic term for the CC-Link IE Controller Network module and CC-Link IE Field Network module
MELSECNET/H module	An abbreviation for the MELSECNET/H network module
Ethernet module	An abbreviation for the Ethernet interface module
CC-Link module	An abbreviation for the CC-Link system master/local module
■ Network	
CC-Link IE	A generic term for the CC-Link IE Controller Network and CC-Link IE Field Network
MELSECNET/H	An abbreviation for the MELSECNET/H network system
■ Memory extension	
Memory card	A generic term for SRAM card, Flash card, and ATA card
SRAM card	A generic term for the Q2MEM-1MBSN, Q2MEM-1MBS, Q2MEM-2MBSN, Q2MEM-2MBS, Q3MEM-4MBS, and Q3MEM-8MBS SRAM cards
Flash card	A generic term for the Q2MEM-2MBF and Q2MEM-4MBF Flash cards
ATA card	A generic term for the Q2MEM-8MBA, Q2MEM-16MBA, and Q2MEM-32MBA ATA cards
SD memory card	A generic term for the L1MEM-2GBSD and L1MEM-4GBSD SD Secure Digital memory cards. An SD card is a non-volatile memory card.
Extended SRAM cassette	A generic term for the Q4MCA-1MBS, Q4MCA-2MBS, Q4MCA-4MBS, and Q4MCA-8MBS extended SRAM cassettes
■ Software package	
Programming tool	A generic term for GX Works2 and GX Developer
GX Works2	The product name for the MELSEC programmable controller software package
GX Developer	
■ Others	
Control CPU	A CPU module which controls each I/O module and intelligent function module. In a multiple CPU system, the CPU module which executes the control can be set for each module.
Controlled module	I/O modules and intelligent function modules which are controlled by a control CPU

Term	Description
Non-controlled module	I/O modules and intelligent function modules that are controlled by CPU modules other than a control CPU
Extension cable	A generic term for the QC05B, QC06B, QC12B, QC30B, QC50B, and QC100B extension cables
Battery	A generic term for the Q6BAT, Q7BATN, Q7BAT, and Q8BAT CPU module batteries, Q2MEM-BAT SRAM card battery, and Q3MEM-BAT SRAM card battery
QA6ADP	An abbreviation for the QA6ADP QA conversion adapter module
QA1S6ADP	A generic term for the QA1S6ADP and QA1S6ADP-S1 Q-AnS base unit conversion adapter
GOT	A generic term for Mitsubishi Electric Graphic Operation Terminal, GOT-A*** series, GOT-F*** series, and GOT1000 series

Memo

CHAPTER 1 OVERVIEW

In a multiple CPU system, more than one CPU module is mounted on the main base unit and each CPU module controls I/O modules and intelligent function modules separately.
QCPUs, Motion CPUs, C Controller modules, and PC CPU modules can be used in multiple CPU systems.
(☞Page 33, CHAPTER 3)



Remark

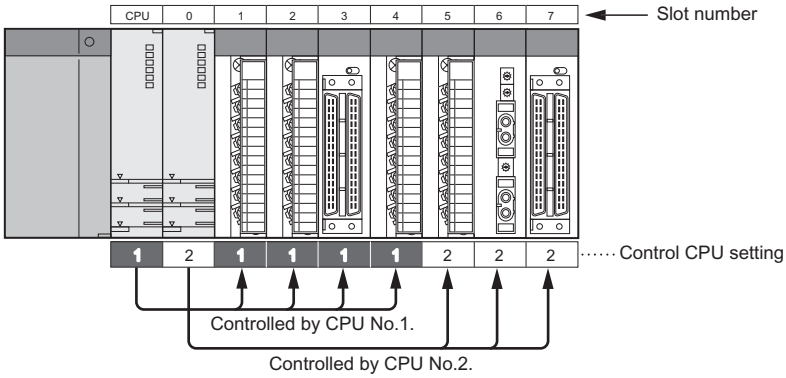
This manual describes the combinations of CPU modules and communications among CPU modules in a multiple CPU system. For the uses, functions, and instruction availabilities of each CPU module, refer to the following.

Manual for the CPU module used

For PC CPU modules, contact CONTEC Co., Ltd.
www.contec.com

(1) Distributed control

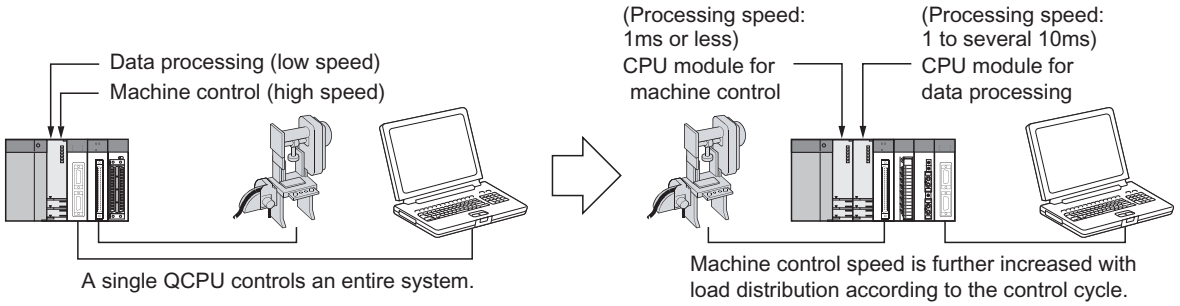
In a multiple CPU system, control can be distributed by specifying a control CPU module for each I/O module and intelligent function module. (☞Page 26, Section 2.1)



Distributed control provides the advantages listed on the following page.

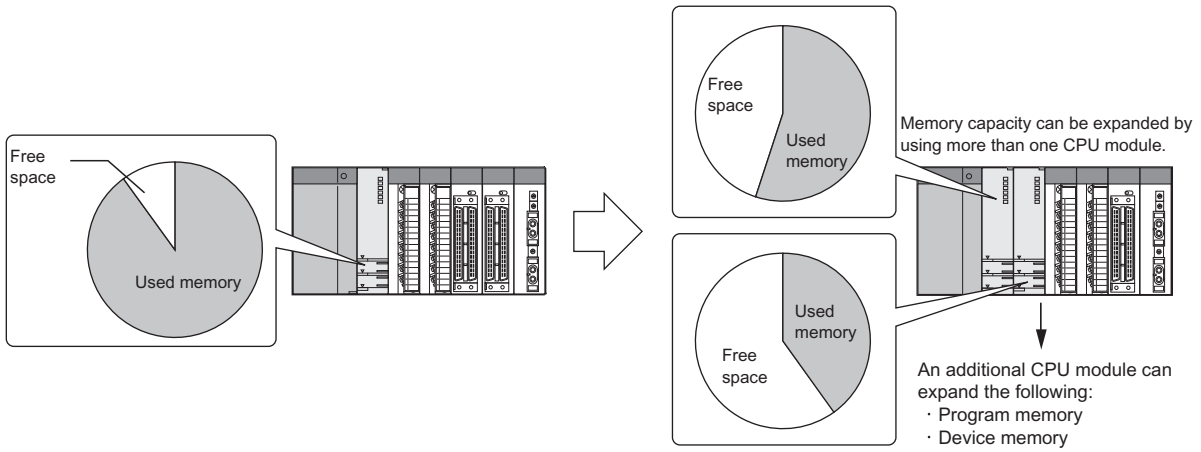
(a) Distribution of processing

The overall system scan time can be reduced by distributing the high-load processing performed in a single CPU module over multiple CPU modules.



(b) Distribution of memory

The memory capacity used for the entire system can be increased by distributing the memory areas over multiple CPU modules.

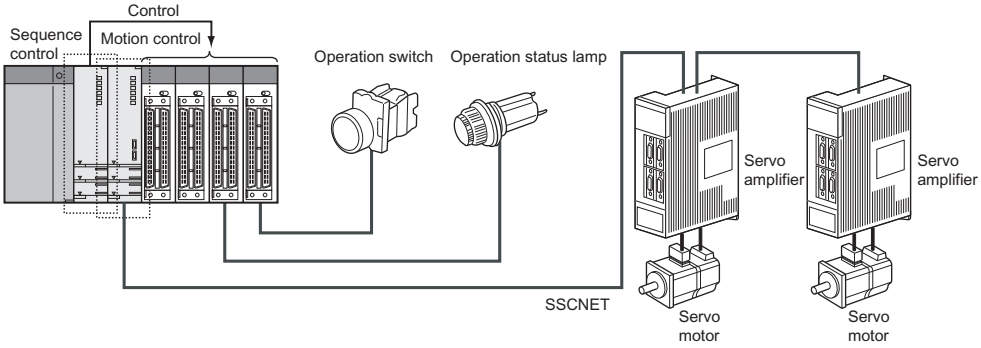


(c) Distribution of functions

Programs can be developed easily by distributing the functions, for example, having different CPU modules control production line A and production line B.

(2) Configuring sequence control and motion control systems on the same base unit

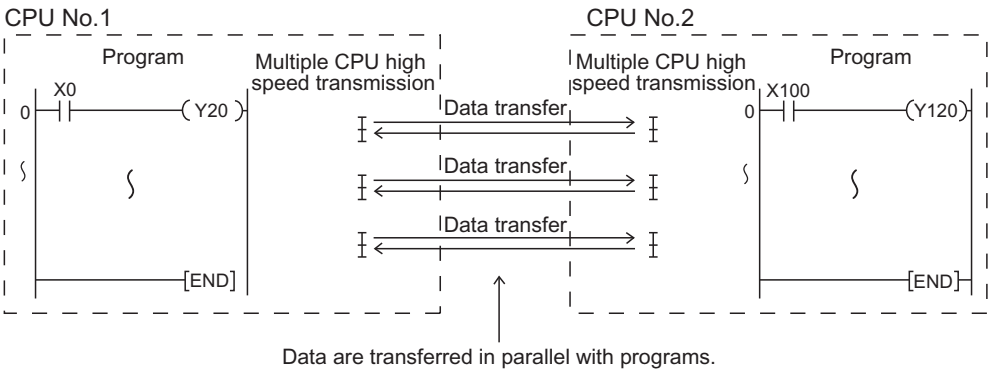
In a multiple CPU system consisting of a QCPU and Motion CPU, sequence control and motion control can be implemented together to achieve a high-level motion system.



Interaction with Motion CPUs for motion control is enhanced in Universal model QCPUs.

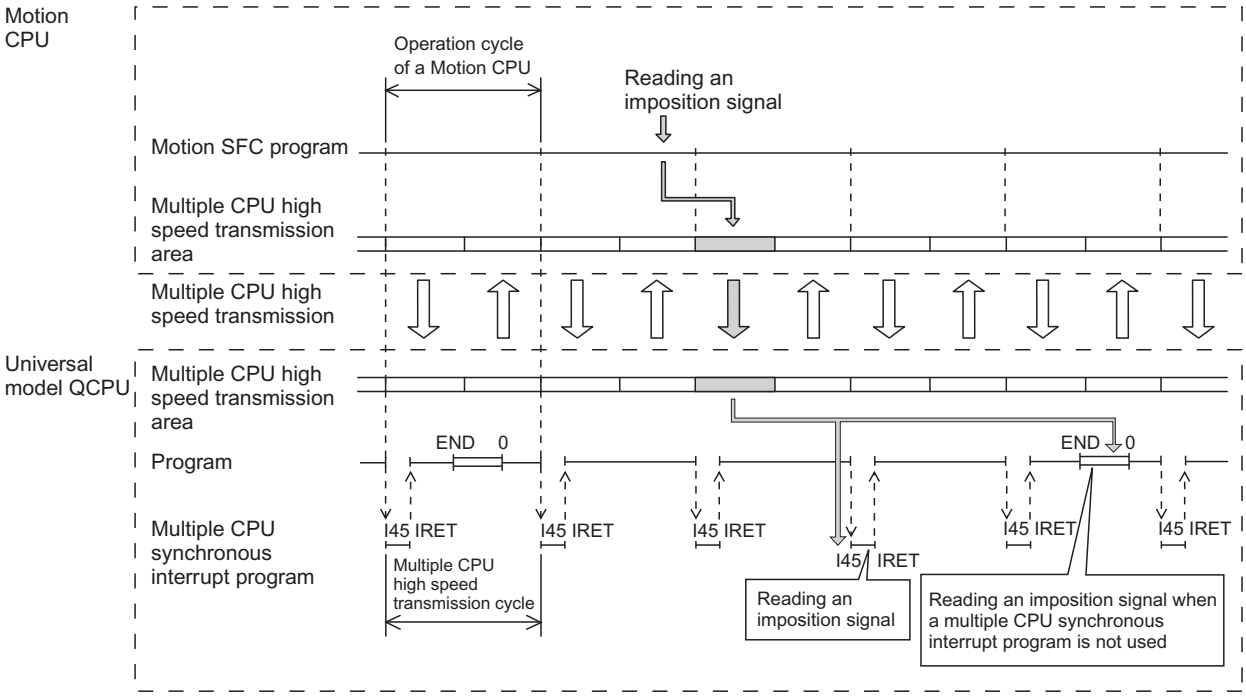
(a) High-speed data transfer between CPU modules

In a multiple CPU system, up to 14K-word data are transferred in parallel with programs between CPU modules. This enables high-speed data transfer independent of scan time, and shortens the takt time of the entire system. (☞Page 153, Section 6.1.3)



(b) Synchronous processing with a motion control

An interrupt program which is synchronized with the operation cycle of a Motion CPU (multiple CPU synchronous interrupt program) can be executed. Command input or output from a Motion CPU can be synchronized with the operation cycle of the Motion CPU, which enables high-speed data transfer independent of scan time. (☞Page 169, Section 6.4)

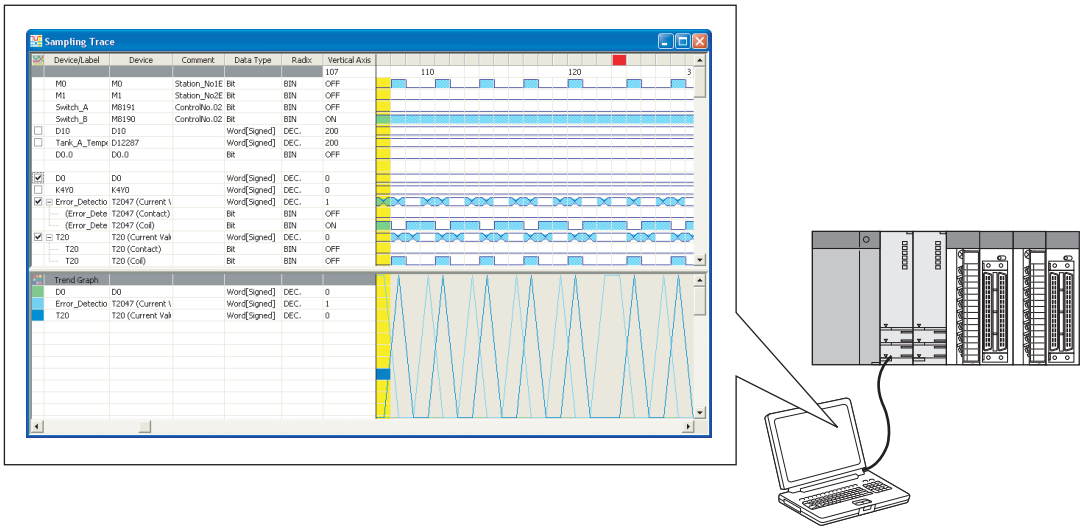


(c) Checking data send/receive timing between CPU modules

With the sampling trace function of Universal model QCPUs, the data communications timing with a Motion CPU can be checked. Timing can also be checked between Universal model QCPUs.

The sampling trace function facilitates the processing for checking the data send/receive timing between CPU modules, and reduces the time for debugging the multiple CPU system.

Sampling trace result display using a programming tool



Point

The sampling trace of other CPU modules in the multiple CPU system can be executed, by specifying the following CPU modules.

- Universal model QCPU (except the Q00UCPU, Q01UCPU, and Q02UCPU)
- Motion CPU (Q172DCPU(-S1), Q173DCPU(-S1), Q172DSCPU, or Q173DSCPU)

(3) Data communications among CPU modules

The following data communications can be performed among CPU modules in a multiple CPU system.

(a) Transferring data among CPU modules

Data can be transferred among CPU modules by setting auto refresh using a programming tool.

(☞Page 125, Section 6.1.1 to Page 138, Section 6.1.2)

(b) Reading data from other CPU modules

Each CPU module can read data from other CPU modules whenever required using the following instructions.

(☞Page 153, Section 6.1.3)

- Read instruction from the CPU shared memory in another CPU module
- Cyclic transmission area device (U3En\G□)

(c) Directing control to the Motion CPU

The QCPU can direct control to the Motion CPU using the following instruction. (☞Page 163, Section 6.2)

- Motion dedicated instruction

(d) Reading/writing device data to/from the Motion CPU

The QCPU can read/write device data to/from the Motion CPU using the following instructions.

(☞Page 165, Section 6.3.1)

- Multiple CPU transmission dedicated instruction
- Multiple CPU high-speed transmission dedicated instruction

(e) Issuing events to the C Controller module or PC CPU module

The QCPU can issue events to the C Controller module or PC CPU module using the following instruction.

(☞Page 167, Section 6.3.2)

- Multiple CPU transmission dedicated instruction

The Universal model QCPU (except the Q00UCPU, Q01UCPU, and Q02UCPU) can execute the motion dedicated instruction multiple times in one scan. Since the motion dedicated instruction can be executed consecutively to different axis numbers, delay time of servo startup intervals can be shortened.

(f) Logging communication data among CPU modules

Communication data among CPU modules can be saved to an SD memory card in CSV format by logging the cyclic transmission area device (U3EnG□) using the data logging function of the CPU module.

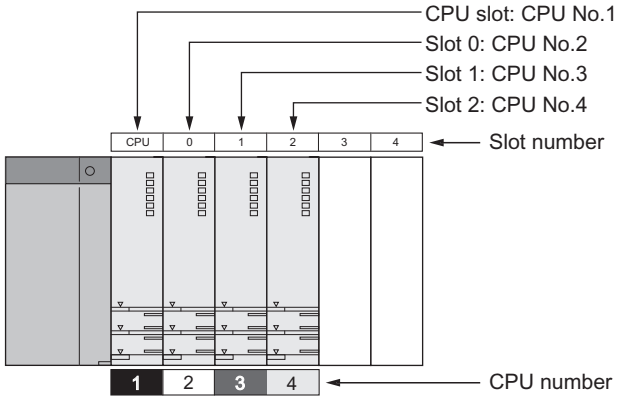
The High-speed Universal model QCPU and Universal model Process CPU support the data logging function.

(QnUDVCPU/LCPU User's Manual (Data Logging Function))

CHAPTER 2 CONCEPT OF MULTIPLE CPU SYSTEM

2.1 CPU Numbers

CPU numbers are assigned to identify CPU modules contained in a multiple CPU system.
A CPU module mounted in the CPU slot of a main base unit will be CPU No.1. CPU No.2, No.3, and No.4 will be assigned sequentially to the right of CPU No.1.



(1) Available CPU numbers

Available CPU numbers differ depending on the QCPU used as CPU No.1 and the main base unit used.
(☞ Page 33, CHAPTER 3)

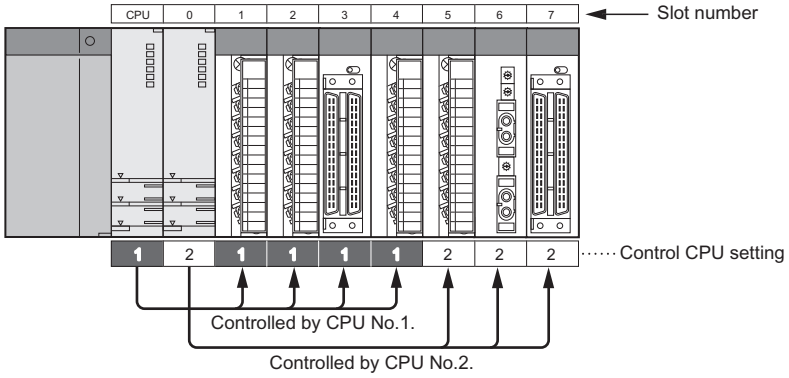
Ex. When a Basic model QCPU is used as CPU No.1, the total number of mountable CPU modules is three (CPU No.1 to No.3). However, when a slim type main base unit (Q3□SB) or multiple CPU high-speed main base unit (Q3□DB) is used, the number of mountable CPU modules is limited to one or two (CPU No.1 and No.2).

(2) Uses of CPU numbers

CPU numbers are used for the following purposes.

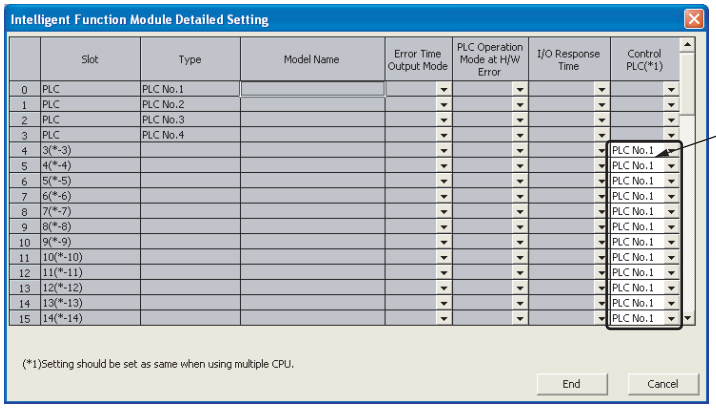
(a) Setting control CPUs

CPU numbers are used to set a control CPU for each I/O module and intelligent function module.



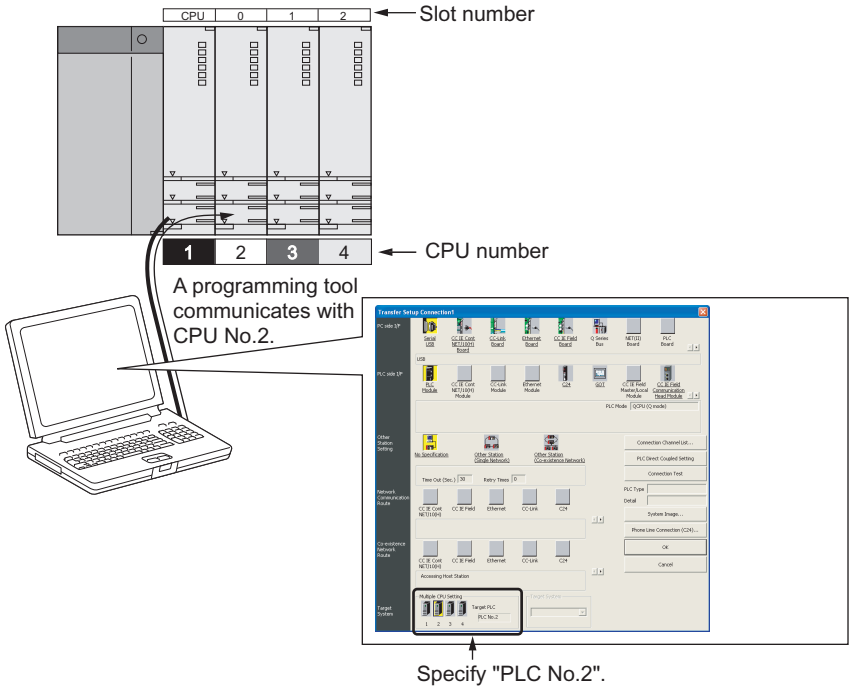
Set control CPUs in PLC parameter ("I/O Assignment").

Project window ⇨ [Parameter] ⇨ [PLC Parameter] ⇨ [I/O Assignment] ⇨ Detailed Setting



(b) Specifying a connection target using a programming tool (personal computer)

CPU numbers are used to specify a CPU module to which a programming tool is connected.

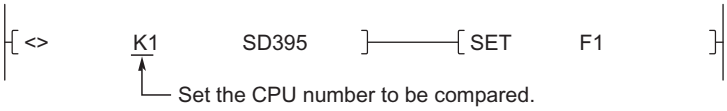


(3) Checking the host CPU number

The host CPU number of a QCPU is stored in SD395 (Multiple CPU system information). A host CPU number check program (refer to an example below) should be created. If created, the following status can be checked easily.

- Incorrect mounting status of the QCPU
- Program writing status to other CPU modules using the programming tool

In the following program, if the QCPU to which the program is written is other than CPU No.1 (if the value in SD395 is other than "1"), the annunciator (F1) turns on. Accordingly, the USER LED of the QCPU turns on. The corresponding annunciator number is stored in SD62 (Annunciator number).



2.2 I/O Number Assignment

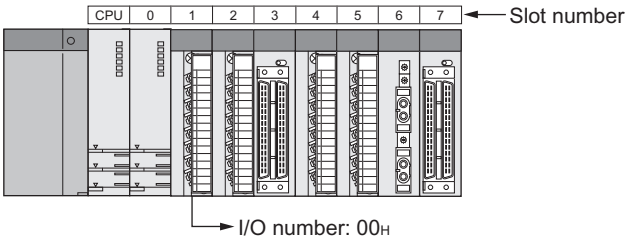
A multiple CPU system uses the following two I/O numbers.

- I/O numbers used by CPU modules to communicate with I/O modules and intelligent function modules (☞Page 29, Section 2.2.1)
- I/O numbers used by CPU modules to communicate with other CPU modules (☞Page 32, Section 2.2.2)

2.2.1 I/O numbers of I/O modules and intelligent function modules

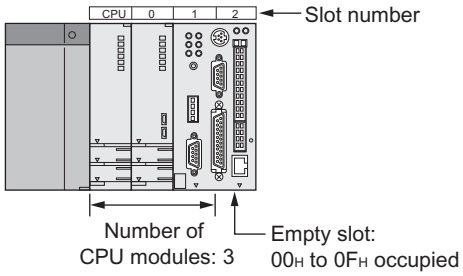
In the same way as in single CPU systems, I/O number "00_H" is assigned to the I/O module or intelligent function module mounted to the right of the CPU module. The subsequent I/O numbers are assigned sequentially to the right. In multiple CPU systems, however, CPU modules may be mounted in slots 0 to 2 as well, and accordingly the start slot of "00_H" varies.

Ex. When two CPU modules are mounted

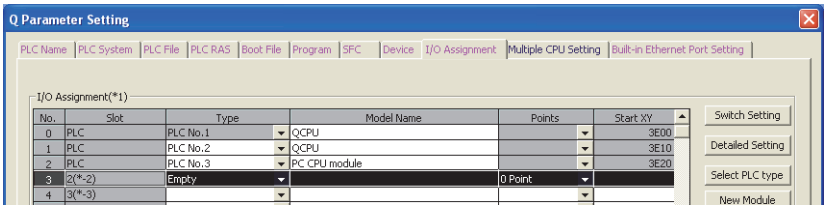


Point

- Some CPU modules occupy two or more slots. When this type of CPU module is used, the second slot and after are treated as empty slots.
  In the case of a PC CPU module, for example, the right slot of the occupied two slots is treated as an empty slot having 16 points. (An empty slot occupies 16 points by default.)
  For this reason, the start I/O number of the module mounted on the right of the PC CPU module will be "10_H".



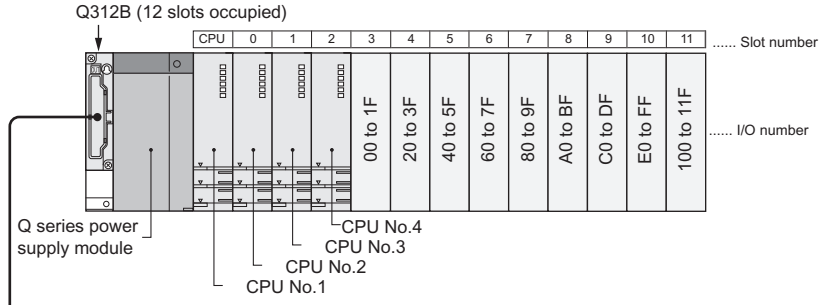
  Note that the start I/O number can be changed to "00_H" by setting "0 Point" to the number of points for the right slot of the PC CPU module in PLC parameter ("I/O Assignment").



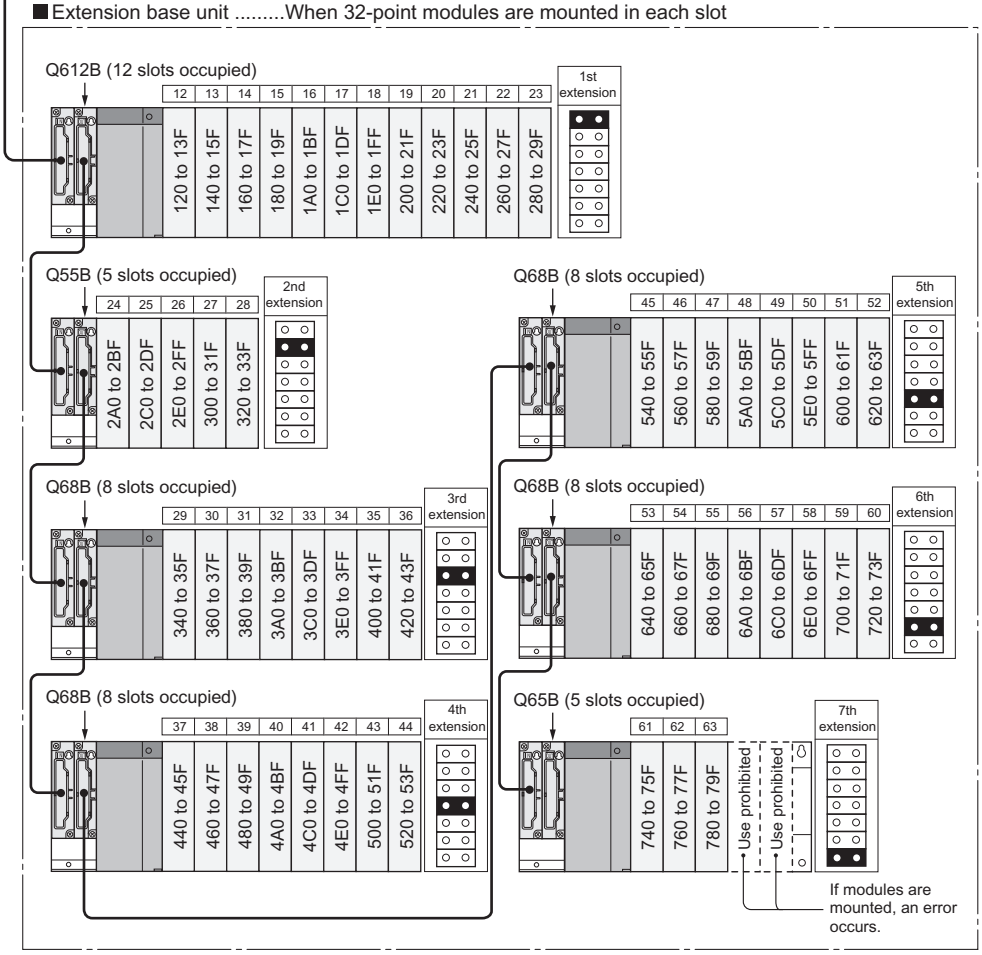
- The I/O numbers of the multiple CPU system can be checked on the System monitor window using a programming tool.
- In the same way as in single CPU systems, the position of I/O number "00_H" can be changed to any slot in PLC parameter ("I/O Assignment"). (User's Manual (Function Explanation, Program Fundamentals) for the CPU module used)

Ex. Example of I/O number assignment

■Main base unit.....When 32-point modules are mounted in each slot



■Extension base unit .....When 32-point modules are mounted in each slot



2.2.2 I/O numbers of CPU modules

In multiple CPU systems, I/O numbers are assigned to each CPU module to specify mounted CPU modules. The I/O number for each CPU module is fixed at the corresponding slot, and cannot be changed in PLC parameter ("I/O Assignment").
The following is the list of I/O numbers that can be assigned to CPU modules.

Item	CPU module mounting position			
	CPU slot	Slot 0	Slot 1	Slot 2
Start I/O number	$3E00_H$	$3E10_H$	$3E20_H$	$3E30_H$

Available slots differ depending on the QCPU used as CPU No.1 and the main base unit used. (☞Page 33, CHAPTER 3)

(1) Uses of I/O numbers of CPU modules

The I/O numbers of CPU modules are used for the following purposes.

- Communications among CPU modules (☞Page 119, CHAPTER 6)
- Specifying the communication-target CPU module under the MC protocol (MELSEC-Q/L MELSEC Communication Protocol Reference Manual)

CHAPTER 3 SYSTEM CONFIGURATION

In a multiple CPU system, QCPUs, motion CPUs, C Controller modules, and PC CPU modules can be mounted in the CPU slot to slot 2 of the main base unit.
I/O modules and intelligent function modules are mounted to the right of CPU modules.

This chapter describes the system configurations according to the QCPU used as CPU No.1.

Remark

- For a multiple CPU system using a C Controller module as CPU No.1, refer to the manual for the C Controller module used.
- For PC CPU modules, contact CONTEC Co., Ltd.
  www.contec.com

3.1 System Using Basic Model QCPU as CPU No.1

This section describes the system configuration using a Basic model QCPU as CPU No.1.

3.1.1 Available CPU modules, base units, power supply modules, and extension cables

Available CPU modules and the number of mountable modules differ depending on the main base unit used.

(1) When a main base unit (Q3□B) is used

(a) Available modules, the number of extension base units, and the number of mountable modules

Item	Description		
Number of CPU modules	3 CPU modules CPU No.1 (Basic model QCPU) CPU No.2 (Motion CPU) CPU No.3 (C Controller module or PC CPU module)		
Applicable CPU module*1	Basic model QCPU	Q00CPU, Q01CPU	Function version B or later
	Motion CPU*2	Q172CPUN(-T), Q173CPUN(-T), Q172HCPU(-T), Q173HCPU(-T)	Manual for the Motion CPU used
	C Controller module	Q06CCPU-V, Q06CCPU-V-B, Q12DCCPU-V, Q24DHCCPU-V, Q24DHCCPU-VG, Q24DHCCPU-LS, Q26DHCCPU-LS	No function version restriction
	PC CPU module	PPC-CPU686(MS)-64, PPC-CPU686(MS)-128, PPC-CPU852(MS)-512	Manual for the PC CPU module used
Maximum number of extension base units	4 extension base units		
Maximum number of mountable I/O modules	25 - (Number of CPU modules)		
Applicable main base unit	Q33B, Q35B, Q38B, Q312B		
Applicable extension base unit	Type requiring no power supply module (Q series)	Q52B, Q55B	
	Type requiring power supply module (Q series)	Q63B, Q65B, Q68B, Q612B	
Applicable extension cable	QC05B, QC06B, QC12B, QC30B, QC50B, QC100B		
Applicable power supply module	Q61P-A1, Q61P-A2, Q61P, Q61P-D, Q62P, Q63P, Q64P, Q64PN		

*1 For the CPU modules that can be combined and their mounting positions, refer to Page 39, Section 3.1.2.

*2 When using a Motion CPU, install operating system software on the CPU module. For models and versions of the operating system, refer to the manual for the Motion CPU used.

(b) Precautions

- If I/O modules are mounted exceeding the maximum number, "SP.UNIT LAY ERR" (error code: 2124) occurs.
- "Number of CPU modules" indicates the number set in "No. of PLC" of PLC parameter ("Multiple CPU Setting").
- When a C Controller module which occupies three slots is used, the maximum number of mountable I/O modules will be two smaller than the number defined in the table on Page 34, Section 3.1.1 (1) (a).
- A PC CPU module occupies two slots. When this module is used, the maximum number of mountable I/O modules will be one smaller than the number defined in the table on Page 34, Section 3.1.1 (1) (a).

(2) When a redundant power main base unit (Q3□RB) is used

(a) Available modules, the number of extension base units, and the number of mountable modules

Item	Description		
Number of CPU modules	2 CPU modules CPU No.1 (Basic model QCPU) CPU No.2 (C Controller module)		
Applicable CPU module[*1]	Basic model QCPU	Q00CPU, Q01CPU	Function version B or later
	C Controller module	Q24DHCCPU-V, Q24DHCCPU-VG, Q24DHCCPU-LS, Q26DHCCPU-LS	No function version restriction
Maximum number of extension base units	4 extension base units		
Maximum number of mountable I/O modules	25 - (Number of CPU modules)		
Applicable main base unit	Q38RB		
Applicable extension base unit	Type requiring no power supply module (Q series)	Q52B, Q55B	
	Redundant power extension base unit	Q68RB	
Applicable extension cable	QC05B, QC06B, QC12B, QC30B, QC50B, QC100B		
Applicable power supply module	Q63RP, Q64RP (The Q63RP and Q64RP can be mounted on the same redundant power supply base unit.)		

(b) Precautions

- If I/O modules are mounted exceeding the maximum number, "SP.UNIT LAY ERR" (error code: 2124) occurs.
- "Number of CPU modules" indicates the number set in "No. of PLC" of PLC parameter ("Multiple CPU Setting").
- When a C Controller module which occupies three slots is used, the maximum number of mountable I/O modules will be two smaller than the number defined in the table on Page 36, Section 3.1.1 (2) (a).

(3) When a slim type main base unit (Q3□SB) is used

(a) Available modules, the number of extension base units, and the number of mountable modules

Item	Description		
Number of CPU modules	2 CPU modules CPU No.1 (Basic model QCPU) CPU No.2 (C Controller module)		
Applicable CPU module*1	Basic model QCPU	Q00CPU, Q01CPU	Function version B or later
	C Controller module	Q06CCPU-V, Q06CCPU-V-B, Q12DCCPU-V	No function version restriction
Maximum number of extension base units	Extension not allowed		
Maximum number of mountable I/O modules	Q32SB	1	
	Q33SB	2	
	Q35SB	4	
Applicable main base unit	Q32SB, Q33SB, Q35SB		
Applicable power supply module	Q61SP		

(b) Precautions

Slim type main base units do not have an extension cable connector. Therefore, no extension base unit or GOT can be bus-connected.

(4) When a multiple CPU high speed main base unit (Q3□DB) is used

(a) Available modules, the number of extension base units, and the number of mountable modules

Item	Description		
Number of CPU modules	2 CPU modules CPU No.1 (Basic model QCPU) CPU No.2 (C Controller module or PC CPU module)		
Applicable CPU module*1	Basic model QCPU	Q00CPU, Q01CPU	Function version B or later
	C Controller module	Q06CCPU-V, Q06CCPU-V-B, Q12DCCPU-V, Q24DHCCPU-V, Q24DHCCPU-VG, Q24DHCCPU-LS, Q26DHCCPU-LS	No function version restriction
	PC CPU module	PPC-CPU686(MS)-64, PPC-CPU686(MS)-128, PPC-CPU852(MS)-512	Manual for the PC CPU module used
Maximum number of extension base units	4 extension base units		
Maximum number of mountable I/O modules	25 - (Number of CPU modules)		
Applicable main base unit	Q35DB, Q38DB, Q312DB		
Applicable extension base unit	Type requiring no power supply module (Q series)	Q52B, Q55B	
	Type requiring power supply module (Q series)	Q63B, Q65B, Q68B, Q612B	
Applicable extension cable	QC05B, QC06B, QC12B, QC30B, QC50B, QC100B		
Applicable power supply module	Q61P-A1, Q61P-A2, Q61P, Q61P-D, Q62P, Q63P, Q64P, Q64PN		

*1 For the CPU modules that can be combined and their mounting positions, refer to Page 39, Section 3.1.2.

(b) Precautions

- If I/O modules are mounted exceeding the maximum number, "SP.UNIT LAY ERR" (error code: 2124) occurs.
- "Number of CPU modules" indicates the number set in "No. of PLC" of PLC parameter ("Multiple CPU Setting").
- When a C Controller module which occupies three slots is used, the maximum number of mountable I/O modules will be two smaller than the number defined in the table on Page 38, Section 3.1.1 (4) (a).
- A PC CPU module occupies two slots. When this module is used, the maximum number of mountable I/O modules will be one smaller than the number defined in the table on Page 38, Section 3.1.1 (4) (a).

3.1.2 CPU module combinations and mounting positions

This section describes the combinations and mounting positions of CPU modules when a Basic model QCPU is used as CPU No.1.

Note that the CPU modules that can be mounted differ depending on the main base unit used. (☞Page 34, Section 3.1.1)

(1) Combinations

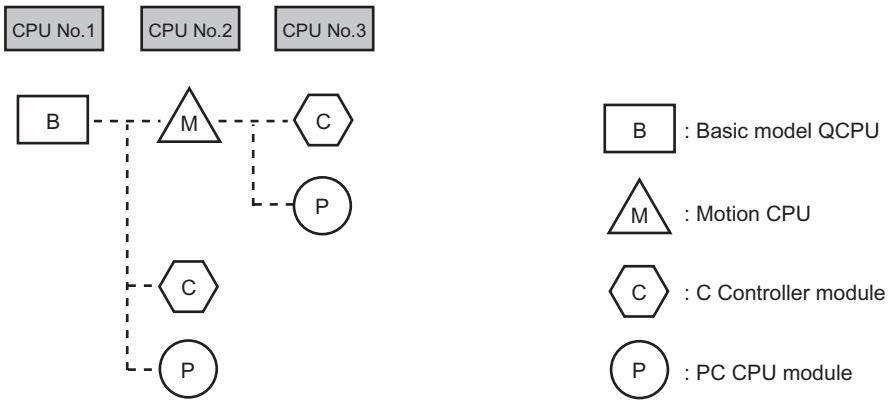
CPU No.1	Number of CPU modules that can be mounted as CPU No.2 or others					Maximum number of mountable modules (including CPU No.1)
	High Performance model QCPU, Process CPU, Universal model QCPU	Motion CPU		C Controller module*1*2	PC CPU module*1	
		Q172CPUN(-T), Q173CPUN(-T), Q172HCPU(-T), Q173HCPU(-T)*2	Q172DCPU(-S1), Q173DCPU(-S1), Q172DSCPU, Q173DSCPU	Q06CCPU-V, Q06CCPU-V-B, Q12DCCPU-V, Q24DHCCPU-V, Q24DHCCPU-VG, Q24DHCCPU-LS, Q26DHCCPU-LS	PPC-CPU686(MS)-64, PPC-CPU686(MS)-128, PPC-CPU852(MS)-512	
Basic model QCPU	Cannot be used together.	0 to 1	Cannot be used together.	0 to 1	0 to 1	3

*1 A C Controller module and a PC CPU module cannot be mounted on the same main base unit.

*2 A C Controller module (Q12DCCPU-V, Q24DHCCPU-V, Q24DHCCPU-VG, Q24DHCCPU-LS, or Q26DHCCPU-LS) and a Motion CPU (Q172CPUN(-T), Q173CPUN(-T), Q172HCPU(-T), or Q173HCPU(-T)) cannot be mounted on the same main base unit.

(2) Mounting positions

The following shows the possible combinations of mounting positions of CPU modules in a multiple CPU system.



(a) Basic model QCPU

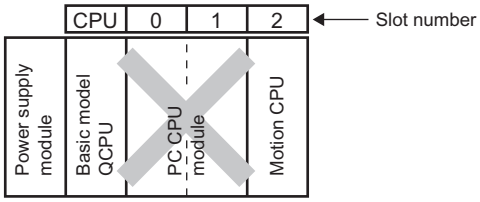
Only one Basic model QCPU can be mounted in the CPU slot (the slot on the right of the power supply module) of the main base unit.

(b) Motion CPU

Only one Motion CPU can be mounted in slot 0 on the right of the Basic model QCPU. It cannot be mounted in a slot other than slot 0.

(c) C Controller module or PC CPU module

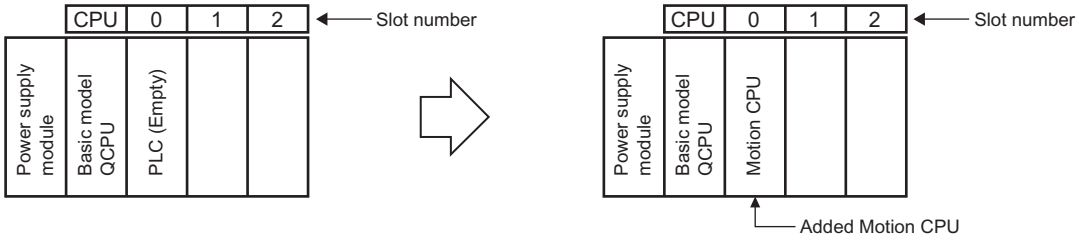
Either a C Controller module or PC CPU module can be mounted on the extreme right of the other CPU module(s). No CPU module can be mounted on the right of the C Controller module or PC CPU module.



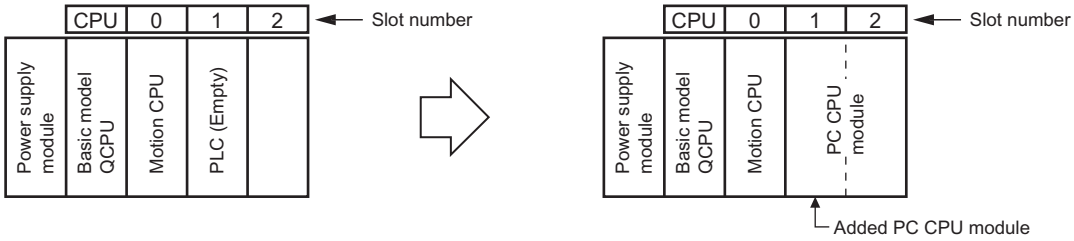
(d) Empty slot setting

Empty slots can be reserved for future addition of CPU modules. Set the number of CPU modules including empty slots in "No. of PLC" of PLC parameter ("Multiple CPU Setting"). Then, set "PLC (Empty)" to the type of a target slot in PLC parameter ("I/O Assignment").

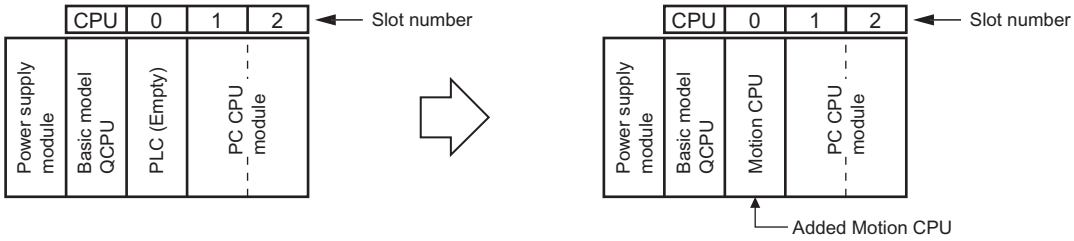
Ex. Adding a Motion CPU in slot 0 in the future



Ex. Adding a PC CPU module in slot 1 in the future



Ex. Setting "PLC (Empty)" between CPU modules



Point

- When a Basic model QCPU is used, "PLC (Empty)" can be set between CPU modules. This is useful when adding a Motion CPU to the system where a Basic model QCPU and a C Controller module or PC CPU module are used. No program modification is required because the CPU number of the C Controller module or PC CPU module does not need to be changed even after the new module is added.
- For a CPU module that occupies two slots or more, secure as many empty slots as needed for the module.

3.1.3 Available I/O modules and intelligent function modules

This section describes I/O modules and intelligent function modules that can be used.

(1) I/O modules and interrupt module

I/O modules (QX□ and QY□) and interrupt module (QI60) can be used. Any CPU module can be set as a control CPU.

(2) Intelligent function modules

Intelligent function modules with function version B or later can be used. Any CPU module can be set as a control CPU.

Write parameters of each intelligent function module to the CPU module to be controlled.

The following modules can be used even if their function version is not B or later.

Module that can be used even if its function version is not B or later	Description
High-speed counter module (QD62, QD62D, QD62E)	Modules with function version A can be used. Any CPU module can be set as a control CPU.

Remark

Intelligent function modules with function version A (except high-speed counter modules (QD62, QD62D, and QD62E)) can be used in the multiple CPU system only when CPU No.1 is set as a control CPU.

- External devices can access only the control CPU (CPU No.1) via a serial communication module.
- External devices cannot access CPU modules other than the control CPU (CPU No.1) via a MELSECNET/H module or serial communication module.
- If any of CPU No.2 to No.4 is set as a control CPU, "SP.UNIT VER.ERR" (error code: 2150) will occur and the multiple CPU system will not start up.

(3) Number of mountable modules

Refer to Page 71, Section 3.5.

(4) Access ranges of controlled and non-controlled modules

Each CPU module can access non-controlled modules by setting "I/O Sharing When Using Multiple CPUs" in PLC parameter ("Multiple CPU Setting"). (☞Page 107, Section 5.2)

Point

If all of the following conditions are met, use a MELSECNET/H module with a serial number (first five digits) of "10042" or later.

- A multiple CPU system containing a Built-in Ethernet port QCPU is configured.
- A programming tool or GOT is connected to an Ethernet port of the Built-in Ethernet port QCPU.
- A programming tool or GOT accesses another station via a MELSECNET/H module controlled by a CPU module other than the control CPU.
- The access target on another station is an A/QnA series CPU module.

3.2 System Using High Performance Model QCPU or Process CPU as CPU No.1

This section describes the system configuration using a High Performance model QCPU or Process CPU as CPU No.1.

3.2.1 Available CPU modules, base units, power supply modules, and extension cables

Available CPU modules and the number of mountable modules differ depending on the main base unit used.

(1) When a main base unit (Q3□B) is used

(a) Available modules, the number of extension bases units, and the number of mountable modules

Item	Description		
Number of CPU modules	4 CPU modules		
Applicable CPU module*1	High Performance model QCPU	Q02(H)CPU, Q06HCPU, Q12HCPU, Q25HCPU	• Function version B • Function version B with a serial number (first five digits) of "03051" or later when used as CPU No.1 and with a PC CPU module
	Process CPU	Q02PHCPU, Q06PHCPU, Q12PHCPU, Q25PHCPU	No function version restriction
	Universal model QCPU	Q03UD(E)CPU, Q03UDVCPU, Q04UD(E)HCPU, Q04UDVCPU, Q04UDPVCPU, Q06UD(E)HCPU, Q06UDVCPU, Q06UDPVCPU, Q10UD(E)HCPU, Q13UD(E)HCPU, Q13UDVCPU, Q13UDPVCPU, Q20UD(E)HCPU, Q26UD(E)HCPU, Q26UDVCPU, Q26UDPVCPU, Q50UDEHCPU, Q100UDEHCPU	No function version restriction
	Motion CPU*2	Q172CPUN(-T), Q173CPUN(-T), Q172HCPU(-T), Q173HCPU(-T)	Manual for the Motion CPU used
	C Controller module	Q06CCPU-V, Q06CCPU-V-B	• Serial number (first five digits) of "10012" or later when used with the Q03UDECPU, Q04UDEHCPU, Q06UDEHCPU, Q13UD(E)HCPU, or Q26UD(E)HCPU • Serial number (first five digits) of "10102" or later when used with the Q10UD(E)HCPU, Q20UD(E)HCPU, Q50UDEHCPU, or Q100UDEHCPU • Cannot be used with the QnUDVCPU and QnUDPVCPU.
		Q12DCCPU-V	• Serial number (first five digits) of "14122" or later when used with the QnUDVCPU • Cannot be used with the QnUDPVCPU.
		Q24DHCCPU-V	• Serial number (first five digits) of "14122" or later when used with the QnUDVCPU • Serial number (first five digits) of "15051" or later when used with the QnUDPVCPU

Item	Description		
Applicable CPU module[*1]	C Controller module	Q24DHCCPU-VG, Q24DHCCPU-LS, Q26DHCCPU-LS	No function version restriction
	PC CPU module	PPC-CPU686(MS)-64, PPC-CPU686(MS)-128, PPC-CPU852(MS)-512	Manual for the PC CPU module used Cannot be used with the QnUDVCPU and QnUDPVCPU.
Maximum number of extension base units	7 extension base units		
Maximum number of mountable I/O modules	65 - (Number of CPU modules)		
Applicable main base unit	Q33B, Q35B, Q38B, Q312B		
Applicable extension base unit	Type requiring no power supply module (Q series)	Q52B, Q55B	
	Type requiring power supply module (Q series)	Q63B, Q65B, Q68B, Q612B	
	Type requiring no power supply module (AnS series)[*3*4]	QA1S51B, QA1S6ADP+A1S5□B[*6]	
	Type requiring power supply module (AnS series)[*3*5]	QA1S65B, QA1S68B, QA1S6ADP+A1S6□B[*6]	
	Type requiring no power supply module (A series)[*3]	QA6ADP+A5□B	
	Type requiring power supply module (A series)[*3]	QA65B, QA68B, QA6ADP+A6□B	
Applicable extension cable	QC05B, QC06B, QC12B, QC30B, QC50B, QC100B		
Applicable power supply module	Power supply module (Q series)	Q61P-A1, Q61P-A2, Q61P, Q61P-D, Q62P, Q63P, Q64P, Q64PN	
	Power supply module (AnS series)[*3]	A1S61PN, A1S62PN, A1S63P	
	Power supply module (A series)[*3]	A61P, A61PN, A62P, A63P, A61PEU, A62PEU	

*1 For the CPU modules that can be combined and their mounting positions, refer to Page 49, Section 3.2.2.

*2 When using a Motion CPU, install operating system software on the CPU module. For models and versions of the operating system, refer to the manual for the Motion CPU used.

*3 These units and modules cannot be used in a multiple CPU system including a Process CPU and a Universal model Process CPU. (☞ Page 191, Appendix 3)

*4 Since the QA1S51B does not have an extension cable connector (OUT), it cannot be used with the QA6□B or QA6ADP+A5□B/A6□B.

*5 When the QA1S6□B is used as an extension base unit, the QA6ADP+A5□B/A6□B cannot be connected.

*6 When the QA1S6ADP+A1S5□B/A1S6□B is used, the maximum number of extension base units is 1, and the maximum number of I/O modules that can be mounted is 20 minus the number of CPU modules. When the QA1S6ADP-S1+A1S5□B/A1S6□B is used, the maximum number of extension base units is 3, and the maximum number of I/O modules that can be mounted is 36 minus the number of CPU modules.

(b) Precautions

- Extension base units, QA1S5□B, QA1S6□B, QA1S6ADP+A1S5□B/A1S6□B, QA6□B, and QA6ADP+A5□B/A6□B, can be connected when a High Performance model QCPU is set as the control CPU of AnS/A series modules. (☞ Page 191, Appendix 3)
- If I/O modules are mounted exceeding the maximum number, "SP.UNIT LAY ERR" (error code: 2124) occurs.
- "Number of CPU modules" indicates the number set in "No. of PLC" of PLC parameter ("Multiple CPU Setting").
- When a C Controller module which occupies three slots is used, the maximum number of mountable I/O modules will be two smaller than the number defined in the table on Page 43, Section 3.2.1 (1) (a).
- A PC CPU module occupies two slots. When this module is used, the maximum number of mountable I/O modules will be one smaller than the number defined in the table on Page 43, Section 3.2.1 (1) (a).

(2) When a redundant power main base unit (Q3□RB) is used

(a) Available modules, the number of extension base units, and the number of mountable modules

Item	Description		
Number of CPU modules	4 CPU modules		
Applicable CPU module*1	High Performance model QCPU	Q02(H)CPU, Q06HCPU, Q12HCPU, Q25HCPU	Function version B
	Process CPU	Q02PHCPU, Q06PHCPU, Q12PHCPU, Q25PHCPU	No function version restriction
	Universal model QCPU	Q03UD(E)CPU, Q03UDVCPU, Q04UD(E)HCPU, Q04UDVCPU, Q04UDPVCPU, Q06UD(E)HCPU, Q06UDVCPU, Q06UDPVCPU, Q10UD(E)HCPU, Q13UD(E)HCPU, Q13UDVCPU, Q13UDPVCPU, Q20UD(E)HCPU, Q26UD(E)HCPU, Q26UDVCPU, Q26UDPVCPU, Q50UDEHCPU, Q100UDEHCPU	No function version restriction
	C Controller module	Q24DHCCPU-V	• Serial number (first five digits) of "14122" or later when used with the QnUDVCPU • Serial number (first five digits) of "15051" or later when used with the QnUDPVCPU
		Q24DHCCPU-VG, Q24DHCCPU-LS, Q26DHCCPU-LS	No function version restriction
Maximum number of extension base units	7 extension base units		
Maximum number of mountable I/O modules	65 - (Number of CPU modules)		
Applicable main base unit	Q38RB		
Applicable extension base unit	Type requiring no power supply module (Q series)	Q52B, Q55B	
	Redundant power extension base unit	Q68RB	
Applicable extension cable	QC05B, QC06B, QC12B, QC30B, QC50B, QC100B		
Applicable power supply module	Q63RP, Q64RP (The Q63RP and Q64RP can be mounted on the same redundant power supply base unit.)		

*1 For the CPU modules that can be combined and their mounting positions, refer to Page 49, Section 3.2.2.

(b) Precautions

- If I/O modules are mounted exceeding the maximum number, "SP.UNIT LAY ERR" (error code: 2124) occurs.
- "Number of CPU modules" indicates the number set in "No. of PLC" of PLC parameter ("Multiple CPU Setting").
- When a C Controller module which occupies three slots is used, the maximum number of mountable I/O modules will be two smaller than the number defined in the table on Page 45, Section 3.2.1 (2) (a).

(3) When a slim type main base unit (Q3□SB) is used

(a) Available modules, the number of extension base units, and the number of mountable modules

Item	Description		
Number of CPU modules	3 CPU modules		
Applicable CPU module*1	High Performance model QCPU	Q02(H)CPU, Q06HCPU, Q12HCPU, Q25HCPU	Function version B
	Universal model QCPU	Q03UD(E)CPU, Q03UDVCPU, Q04UD(E)HCPU, Q04UDVCPU, Q06UD(E)HCPU, Q06UDVCPU, Q10UD(E)HCPU, Q13UD(E)HCPU, Q13UDVCPU, Q20UD(E)HCPU, Q26UD(E)HCPU, Q26UDVCPU, Q50UDEHCPU, Q100UDEHCPU	No function version restriction
	C Controller module	Q06CCPU-V, Q06CCPU-V-B	• Serial number (first five digits) of "10012" or later when used with the Q03UDECPU, Q04UDEHCPU, Q06UDEHCPU, Q13UD(E)HCPU, or Q26UD(E)HCPU • Serial number (first five digits) of "10102" or later when used with the Q10UD(E)HCPU, Q20UD(E)HCPU, Q50UDEHCPU, or Q100UDEHCPU • Cannot be used with the QnUDVCPU.
		Q12DCCPU-V	Serial number (first five digits) of "14122" or later when used with the QnUDVCPU
Maximum number of extension base units	Extension not allowed		
Maximum number of mountable I/O modules	Q32SB	3 - (Number of CPU modules)	
	Q33SB	4 - (Number of CPU modules)	
	Q35SB	6 - (Number of CPU modules)	
Applicable main base unit	Q32SB, Q33SB, Q35SB		
Applicable power supply module	Q61SP		

*1 For the CPU modules that can be combined and their mounting positions, refer to Page 49, Section 3.2.2.

(b) Precautions

- Slim type main base units do not have an extension cable connector. Therefore, no extension base unit or GOT can be bus-connected.
- Four CPU modules cannot be mounted because the power consumption of the CPU modules exceeds the rated output current of the power supply module (Q61SP).
  If a C Controller module is used, three CPU modules cannot be mounted.
- "Number of CPU modules" indicates the number set in "No. of PLC" of PLC parameter ("Multiple CPU Setting").

(4) When a multiple CPU high speed main base unit (Q3□DB) is used

(a) Available modules, the number of extension base units, and the number of mountable modules

Item	Description		
Number of CPU modules	4 CPU modules		
Applicable CPU module*1	High Performance model QCPU	Q02(H)CPU, Q06HCPU, Q12HCPU, Q25HCPU	• Function version B • Function version B with a serial number (first five digits) of "03051" or later when a module is used as CPU No.1 and used with a PC CPU module
	Process CPU	Q02PHCPU, Q06PHCPU, Q12PHCPU, Q25PHCPU	No function version restriction
	Universal model QCPU	Q03UD(E)CPU, Q03UDVCPU, Q04UD(E)HCPU, Q04UDVCPU, Q04UDPVCPU, Q06UD(E)HCPU, Q06UDVCPU, Q06UDPVCPU, Q10UD(E)HCPU, Q13UD(E)HCPU, Q13UDVCPU, Q13UDPVCPU, Q20UD(E)HCPU, Q26UD(E)HCPU, Q26UDVCPU, Q26UDPVCPU, Q50UDEHCPU, Q100UDEHCPU	No function version restriction
	C Controller module	Q06CCPU-V, Q06CCPU-V-B	• Serial number (first five digits) of "10012" or later when used with the Q03UDECPU, Q04UDEHCPU, Q06UDEHCPU, Q13UD(E)HCPU, or Q26UD(E)HCPU • Serial number (first five digits) of "10102" or later when used with the Q10UD(E)HCPU, Q20UD(E)HCPU, Q50UDEHCPU, or Q100UDEHCPU • Cannot be used with the QnUDVCPU and QnUDPVCPU.
		Q12DCCPU-V	• Serial number (first five digits) of "14122" or later when used with the QnUDVCPU • Cannot be used with the QnUDPVCPU.
		Q24DHCCPU-V	• Serial number (first five digits) of "14122" or later when used with the QnUDVCPU • Serial number (first five digits) of "15051" or later when used with the QnUDPVCPU
		Q24DHCCPU-VG, Q24DHCCPU-LS, Q26DHCCPU-LS	No function version restriction
	PC CPU module	PPC-CPU686(MS)-64, PPC-CPU686(MS)-128, PPC-CPU852(MS)-512	Manual for the PC CPU module used Cannot be used with the QnUDVCPU and QnUDPVCPU.
Maximum number of extension base units	7 extension base units		
Maximum number of mountable I/O modules	65 - (Number of CPU modules)		
Applicable main base unit	Q35DB, Q38DB, Q312DB		
Applicable extension base unit	Type requiring no power supply module (Q series)	Q52B, Q55B	
	Type requiring power supply module (Q series)	Q63B, Q65B, Q68B, Q612B	
Applicable extension cable	QC05B, QC06B, QC12B, QC30B, QC50B, QC100B		
Applicable power supply module	Q61P-A1, Q61P-A2, Q61P, Q61P-D, Q62P, Q63P, Q64P, Q64PN		

*1 For the CPU modules that can be combined and their mounting positions, refer to Page 49, Section 3.2.2.

(b) Precautions

- If I/O modules are mounted exceeding the maximum number, "SP.UNIT LAY ERR" (error code: 2124) occurs.
- "Number of CPU modules" indicates the number set in "No. of PLC" of PLC parameter ("Multiple CPU Setting").
- When a C Controller module which occupies three slots is used, the maximum number of mountable I/O modules will be two smaller than the number defined in the table on Page 47, Section 3.2.1 (4) (a).
- A PC CPU module occupies two slots. When this module is used, the maximum number of mountable I/O modules will be one smaller than the number defined in the table on Page 47, Section 3.2.1 (4) (a).

3.2.2 CPU module combinations and mounting positions

This section describes the combinations and mounting positions of CPU modules when a High Performance model QCPU or Process CPU is used as CPU No.1.

Note that the CPU modules that can be mounted differ depending on the main base unit used. (☞Page 43, Section 3.2.1)

(1) Combinations

CPU No.1	Number of CPUs that can be mounted as CPU No.2 or others							Maximum number of mountable modules (including CPU No.1)
	High Performance model QCPU, Process CPU, Universal model QCPU*1*2*5*6*7	Motion CPU		C Controller module*3*4*6		PC CPU module*3*5*7		
		Q172CPUN(-T), Q173CPUN(-T), Q172HCPU(-T), Q173HCPU(-T)*2*4	Q172DCPU(-S1), Q173DCPU(-S1), Q172DSCPU, Q173DSCPU	Q06CCPU-V, Q06CCPU-V-B, Q12DCCPU-V	Q24DHCCPU-V, Q24DHCCPU-VG, Q24DHCCPU-LS, Q26DHCCPU-LS	PPC-CPU686(MS)-64, PPC-CPU686(MS)-128	PPC-CPU852(MS)-512	
High Performance model QCPU	0 to 3	0 to 3	Cannot be used together.	0 to 3	0 to 1	0 to 1		4
Process CPU	0 to 3	0 to 3	Cannot be used together.	0 to 3	0 to 1	0 to 1		4

*1 The Q00UCPU, Q01UCPU, and Q02UCPU can be used only as CPU No.1.

*2 A Universal model CPU (except the Q00UCPU, Q01UCPU, and Q02UCPU) and a Motion CPU (Q172CPUN(-T), Q173CPUN(-T), Q172HCPU(-T), or Q173HCPU(-T)) cannot be mounted on the same main base unit.

*3 A C Controller module and a PC CPU module cannot be mounted on the same main base unit.

*4 A C Controller module (Q12DCCPU-V, Q24DHCCPU-V, Q24DHCCPU-VG, Q24DHCCPU-LS, or Q26DHCCPU-LS) and a Motion CPU (Q172CPUN(-T), Q173CPUN(-T), Q172HCPU(-T), or Q173HCPU(-T)) cannot be mounted on the same main base unit.

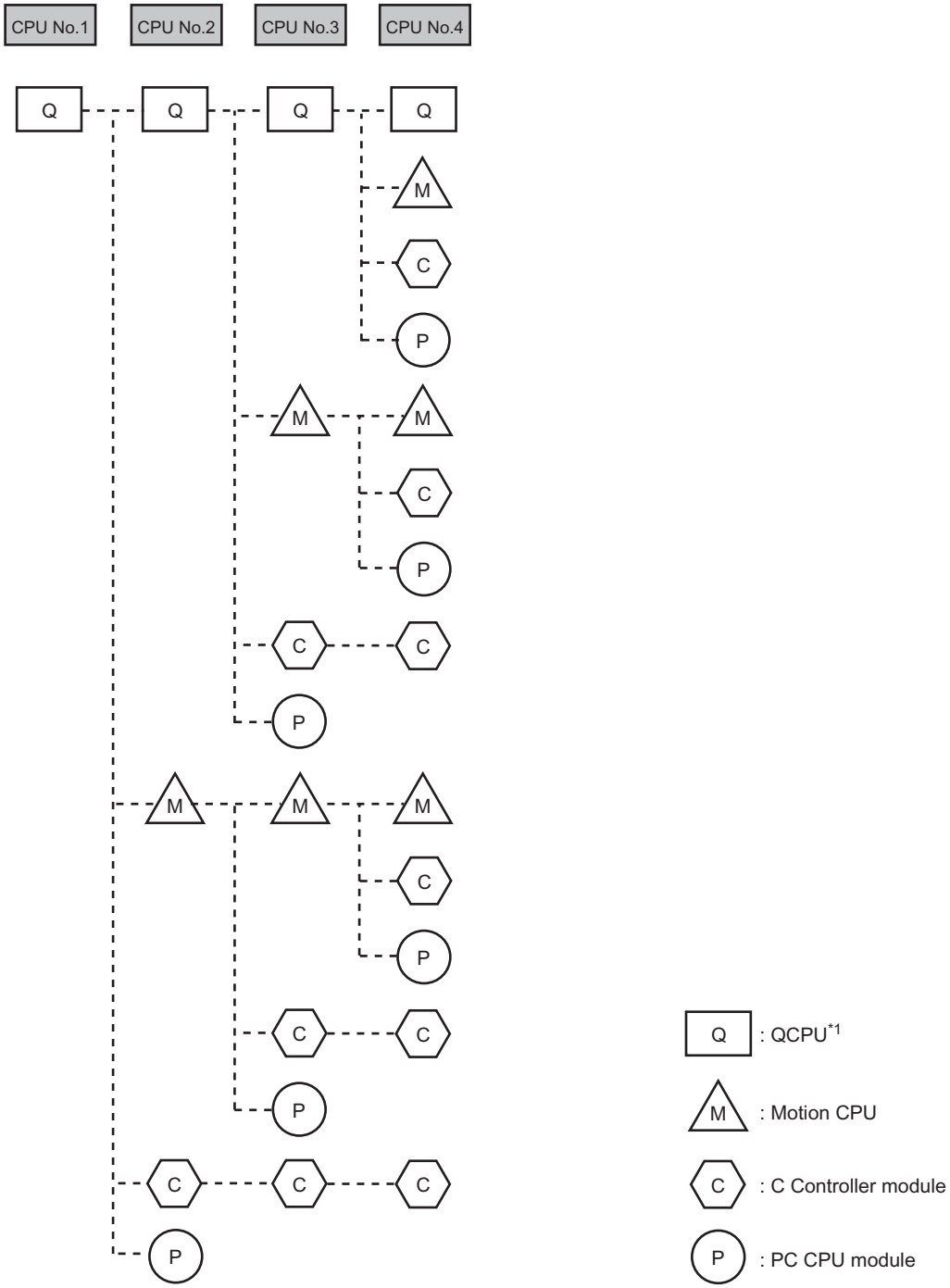
*5 A Universal model QCPU and a PC CPU module (PPC-CPU686(MS)-64 or PPC-CPU686(MS)-128) cannot be used together. When a Universal model QCPU is used, use the PPC-CPU852(MS)-512.

*6 A QnUDVCPU, a QnUDPVCPU, and a C Controller module (Q06CCPU-V or Q06CCPU-V-B) cannot be mounted on the same main base unit.
Also, a QnUDPVCPU and a C Controller module (Q12DCCPU-V) cannot be mounted on the same main base unit.

*7 A QnUDVCPU, a QnUDPVCPU, and a PC CPU module cannot be mounted on the same main base unit.

(2) Mounting positions

The following shows the possible combinations of mounting positions of CPU modules in a multiple CPU system.



*1 The QCPU used as CPU No.1 indicates a High Performance model QCPU or Process CPU.
The QCPU used as CPU No.2 or later indicates a High Performance model QCPU, Process CPU, or Universal model QCPU (except the Q00UCPU, Q01UCPU, and Q02UCPU).

(a) High Performance model QCPU or Process CPU

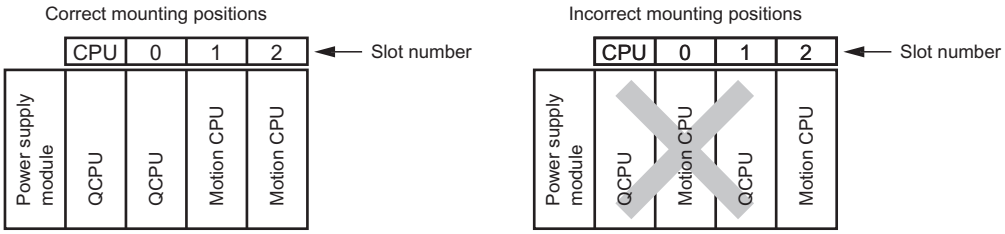
Up to four High Performance model QCPUs and/or Process CPUs can be mounted in the CPU slot (the slot on the right of the power supply module) to slot 2 of the main base unit.

(b) Universal model QCPU

Up to three Universal model QCPUs can be mounted in slot 0 to slot 2 of the main base unit.

(c) Motion CPU

Up to three Motion CPUs can be mounted in the slot on the right of the High Performance model QCPU or Process CPU to slot 2 of the main base unit. Only a Motion CPU, C Controller module, or PC CPU module can be mounted on the right of the Motion CPU.



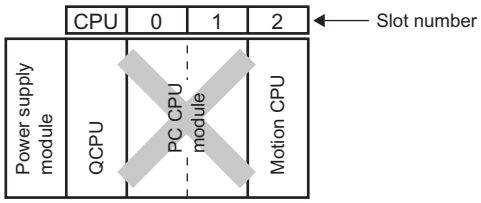
(d) C Controller module

Up to three C Controller modules can be mounted in slot 0 to slot 2 of the main base unit. For a C Controller module which occupies three slots, only one module can be mounted.

Note that only a C Controller module can be mounted on the right of the C Controller module.

(e) PC CPU module

Only one PC CPU module can be mounted on the rightmost slot available for CPU modules. No CPU module can be mounted on the right of the PC CPU module.

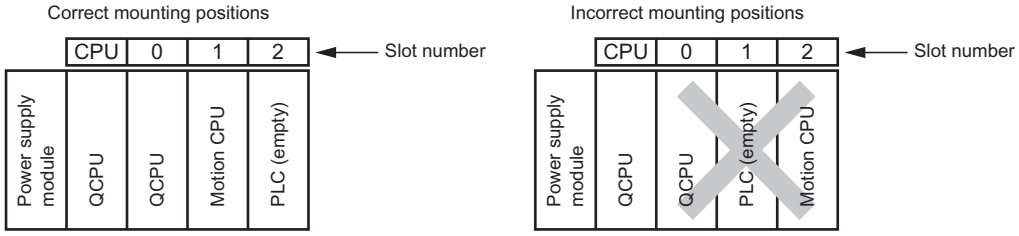


(f) Empty slot setting

Empty slots can be reserved for future addition of CPU modules. Set the number of CPU modules including empty slots in "No. of PLC" of PLC parameter ("Multiple CPU Setting"). Then, set "PLC (Empty)" to the type of a target slot from the right in PLC parameter ("I/O Assignment").

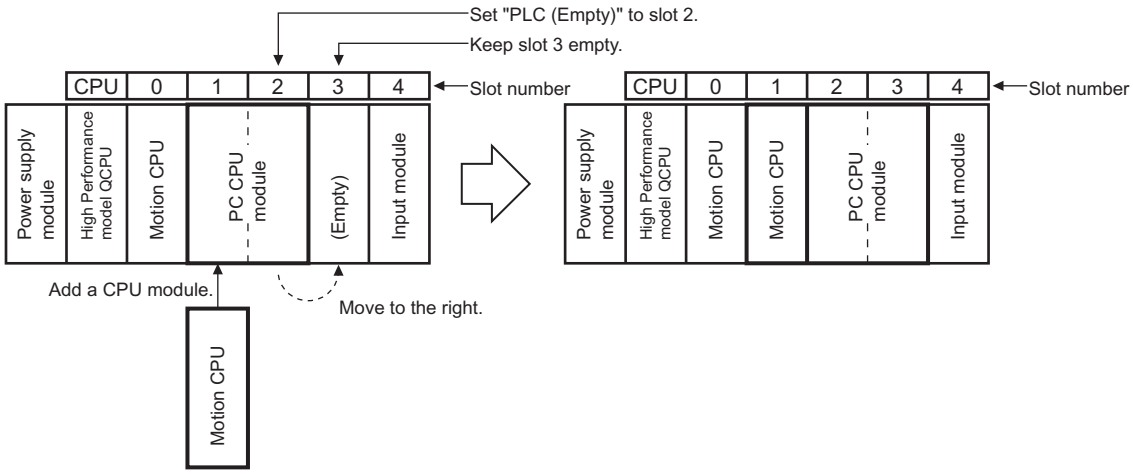
Ex. Setting the number of CPU modules to "4" in PLC parameter and mounting two High Performance model QCPUs and one Motion CPU

Mount the High Performance model QCPUs in the CPU slot and slot 0, and the Motion CPU in slot 1, and set "PLC (Empty)" to slot 2.



Point

When a High Performance model QCPU or Process CPU is used, "PLC (Empty)" cannot be set between CPU modules. To add a CPU module to the system where a C Controller module or PC CPU module is used, move the C Controller module or PC CPU module to the right to allow addition of a CPU module.



3.2.3 Available I/O modules and intelligent function modules

This section describes the I/O modules and intelligent function modules that can be used.

(1) I/O modules, interrupt modules, and intelligent function modules

Refer to the system configuration using a Basic model QCPU as CPU No.1. (☞ Page 42, Section 3.1.3 (1), Page 42, Section 3.1.3 (2))

(2) Modules replaceable online

(a) I/O modules and intelligent function modules that can be replaced

Modules can be replaced online in a multiple CPU system including a Process CPU.
Modules controlled by the Process CPU are targeted.
The following table lists modules that can be replaced online.

Module can be replaced		Restrictions
Input module		No function version restriction
Output module		
I/O combined module		
Intelligent function module	Analog-digital converter module	Function version C
	Digital-analog converter module	
	Temperature input module	
	Temperature control module	
	Pulse input module	
	Load cell input module	
	CT input module	
	Loop control module	

(b) Applicable CPU modules

To replace a module controlled by the Process CPU online, configure a multiple CPU system with the CPU modules listed below.

CPU module	Model	Restrictions
High Performance model QCPU	Q02(H)CPU, Q06HCPU, Q12HCPU, Q25HCPU	Serial number (first five digits) of "04012" or later
Process CPU	Q02PHCPU, Q06PHCPU, Q12PHCPU, Q25PHCPU	No function version restriction
Universal model QCPU	Q03UD(E)CPU, Q03UDVCPU, Q04UD(E)HCPU, Q04UDVCPU, Q04UDPVCPU, Q06UD(E)HCPU, Q06UDVCPU, Q06UDPVCPU, Q10UD(E)HCPU, Q13UD(E)HCPU, Q13UDVCPU, Q13UDPVCPU, Q20UD(E)HCPU, Q26UD(E)HCPU, Q26UDVCPU, Q26UDPVCPU, Q50UDEHCPU, Q100UDEHCPU	
Motion CPU	Q172CPUN(-T), Q173CPUN(-T), Q172HCPU(-T), Q173HCPU(-T)	Version A or later
C Controller module	Q06CCPU-V, Q06CCPU-V-B, Q12DCCPU-V, Q24DHCCPU-V, Q24DHCCPU-VG, Q24DHCCPU-LS, Q26DHCCPU-LS	Manual for the CPU module used
PC CPU module	PPC-CPU686(MS)-64, PPC-CPU686(MS)-128, PPC-CPU852(MS)-512	

(3) Number of mountable modules

Refer to Page 71, Section 3.5.

(4) Access ranges of controlled and non-controlled modules.

Refer to the system configuration using a Basic model QCPU as CPU No.1. (☞Page 42, Section 3.1.3 (4))

3.3 System Using Universal Model QCPU as CPU No.1

This section describes the system configuration using a Universal model QCPU as CPU No.1.

3.3.1 Available CPU modules, base units, power supply modules, and extension cables

Available CPU modules and the number of mountable modules differ depending on the main base unit used.

(1) When a multiple CPU high-speed main base unit (Q3□DB) is used

(a) Available modules, the number of extension base units, and the number of mountable modules

Item	Description		
Number of CPU modules	4 CPU modules		
Applicable CPU module[*1]	Universal model QCPU	Q00UCPU, Q01UCPU, Q02UCPU	The modules can be used as CPU No.1.[*2]
		Q03UD(E)CPU, Q03UDVCPU, Q04UD(E)HCPU, Q04UDVCPU, Q04UDPVCPU, Q06UD(E)HCPU, Q06UDVCPU, Q06UDPVCPU, Q10UD(E)HCPU, Q13UD(E)HCPU, Q13UDVCPU, Q13UDPVCPU, Q20UD(E)HCPU, Q26UD(E)HCPU, Q26UDVCPU, Q26UDPVCPU, Q50UDEHCPU, Q100UDEHCPU	• No function version restriction • Serial number (first five digits) of "09072" or later when used with a PC CPU module
	High Performance model QCPU	Q02(H)CPU, Q06HCPU, Q12HCPU, Q25HCPU	Function version B
	Process CPU	Q02PHCPU, Q06PHCPU, Q12PHCPU, Q25PHCPU	No function version restriction
	Motion CPU[*6]	Q172DCPU(-S1), Q173DCPU(-S1), Q172DSCPU, Q173DSCPU	Manual for the Motion CPU
	C Controller module	Q06CCPU-V, Q06CCPU-V-B	• Serial number (first five digits) of "10102" or later when used with the Q00UCPU, Q01UCPU, or Q02UCPU • Serial number (first five digits) of "10012" or later when used with the Q03UDECPU, Q04UDEHCPU, Q06UDEHCPU, Q13UD(E)HCPU, or Q26UD(E)HCPU • Serial number (first five digits) of "10102" or later when used with the Q10UD(E)HCPU, Q20UD(E)HCPU, Q50UDEHCPU, or Q100UDEHCPU • Cannot be used with the QnUDVCPU and QnUDPVCPU.
		Q12DCCPU-V	• Serial number (first five digits) of "14122" or later when used with the QnUDVCPU • Serial number (first five digits) of "15102" or later and must be in extended mode when used with the QnUDPVCPU
		Q24DHCCPU-V	• Serial number (first five digits) of "14122" or later when used with the QnUDVCPU • Serial number (first five digits) of "15051" or later when used with the QnUDPVCPU
		Q24DHCCPU-VG, Q24DHCCPU-LS, Q26DHCCPU-LS	No function version restriction

Item	Description		
Applicable CPU module[*1]	PC CPU module	PPC-CPU852(MS)-512	• Driver S/W (PPC-DRV-02) version 1.03 or later when used with the Q00UCPU or Q01UCPU • Driver S/W (PPC-DRV-02) version 1.01 or later when used with the Q02UCPU • Driver S/W (PPC-DRV-02) version 1.01 or later when used with the Q03UDCPU, Q04UDHCPU, or Q06UDHCPU • Driver S/W (PPC-DRV-02) version 1.02 or later when used with the Q03UDECPU, Q04UDEHCPU, Q06UDEHCPU, Q13UD(E)HCPU, or Q26UD(E)HCPU • Driver S/W (PPC-DRV-02) version 1.03 or later when used with the Q10UDEHCPU, Q20UDEHCPU, Q50UDEHCPU, or Q100UDEHCPU • Cannot be used with the QnUDVCPU and QnUDPVCPU.
Maximum number of extension base units	7 extension base units, when the Q00UCPU, Q01UCPU, or Q02UCPU is used: 4 extension base units		
Maximum number of mountable I/O modules	65 - (Number of CPU modules), when the Q00UCPU or Q01UCPU is used: 25 - (Number of CPU modules), when the Q02UCPU is used: 37 - (Number of CPU modules)		
Applicable main base unit	Q35DB, Q38DB, Q312DB		
Applicable extension base unit	Type requiring no power supply module (Q series)	Q52B, Q55B	
	Type requiring power supply module (Q series)	Q63B, Q65B, Q68B, Q612B	
	Type requiring no power supply module (AnS series)[*3*5]	QA1S51B, QA1S6ADP+A1S5□B[*7]	
	Type requiring power supply module (AnS series)[*3*4]	QA1S65B, QA1S68B, QA1S6ADP+A1S6□B[*7]	
	Type requiring no power supply module (A series)[*3]	QA6ADP+A5□B	
	Type requiring power supply module (A series)[*3]	QA65B, QA68B, QA6ADP+A6□B	
Applicable extension cable	QC05B, QC06B, QC12B, QC30B, QC50B, QC100B		
Applicable power supply module	Power supply module (Q series)	Q61P-A1, Q61P-A2, Q61P, Q62P, Q63P, Q64P, Q64PN	
	Power supply module (AnS series)[*3]	A1S61PN, A1S62PN, A1S63P	
	Power supply module (A series)[*3]	A61P, A61PN, A62P, A63P, A61PEU, A62PEU	

*1 For the CPU modules that can be combined and their mounting positions, refer to Page 63, Section 3.3.2.

*2 When the Q00UCPU, Q01UCPU, or Q02UCPU is used as CPU No.1, one more CPU module (CPU No.2) can be mounted. The following CPU modules can be mounted as CPU No.2.

CPU module	Model
C Controller module	Q06CCPU-V, Q06CCPU-V-B, Q12DCCPU-V, Q24DHCCPU-V, Q24DHCCPU-VG, Q24DHCCPU-LS, Q26DHCCPU-LS
PC CPU module	PPC-CPU852(MS)-512

*3 These modules and units can be used when a Universal model QCPU with a serial number (first five digits) of "13102" or later is set as the control CPU of AnS/A series modules. These modules and units cannot be used in a multiple CPU system containing a Process CPU and a Universal model Process CPU. (☞ Page 191, Appendix 3)

*4 When the QA1S6□B is used as an extension base unit, the QA6ADP+A5□B/A6□B cannot be connected.

*5 Since the QA1S51B does not have an extension cable connector (OUT), it cannot be used with the QA6□B or QA6ADP+A5□B/A6□B.

*6 When using a Motion CPU, install operating system software on the CPU module. For models and versions of the operating system, refer to the manual for the Motion CPU used.

*7 When the QA1S6ADP+A1S5□B/A1S6□B is used, the maximum number of extension base units is 1, and the maximum number of I/O modules that can be mounted is 20 minus the number of CPU modules. When the QA1S6ADP-S1+A1S5□B/A1S6□B is used, the maximum number of extension base units is 3, and the maximum number of I/O modules that can be mounted is 36 minus the number of CPU modules.

(b) Precautions

- If I/O modules are mounted exceeding the maximum number, "SP.UNIT LAY ERR" (error code: 2124) occurs.
- "Number of CPU modules" indicates the number set in "No. of PLC" of PLC parameter ("Multiple CPU Setting").
- When a C Controller module which occupies three slots is used, the maximum number of mountable I/O modules will be two smaller than the number defined in the table on Page 55, Section 3.3.1 (1) (a).
- A PC CPU module occupies two slots. When this module is used, the maximum number of mountable I/O modules will be one smaller than the number defined in the table on Page 55, Section 3.3.1 (1) (a).

(2) When a main base unit (Q3□B) is used

(a) Available modules, the number of extension base units, and the number of mountable modules

Item	Description		
Number of CPU modules	4 CPU modules		
Applicable CPU module[*1]	Universal model QCPU	Q00UCPU, Q01UCPU, Q02UCPU	The modules can be used as CPU No.1.[*2]
		Q03UD(E)CPU, Q03UDVCPU, Q04UD(E)HCPU, Q04UDVCPU, Q04UDPVCPU, Q06UD(E)HCPU, Q06UDVCPU, Q06UDPVCPU, Q10UD(E)HCPU, Q13UD(E)HCPU, Q13UDVCPU, Q13UDPVCPU, Q20UD(E)HCPU, Q26UD(E)HCPU, Q26UDVCPU, Q26UDPVCPU, Q50UDEHCPU, Q100UDEHCPU	• No function version restriction • Serial number (first five digits) of "09072" or later when used with a PC CPU module
	High Performance model QCPU	Q02(H)CPU, Q06HCPU, Q12HCPU, Q25HCPU	Function version B
	Process CPU	Q02PHCPU, Q06PHCPU, Q12PHCPU, Q25PHCPU	No function version restriction
	Motion CPU	Q172CPUN(-T), Q173CPUN(-T), Q172HCPU(-T), Q173HCPU(-T)	Manual for the Motion CPU Can be used with the Q00UCPU, Q01UCPU, or Q02UCPU.
	C Controller module	Q06CCPU-V, Q06CCPU-V-B	• Serial number (first five digits) of "10102" or later when used with the Q00UCPU, Q01UCPU, or Q02UCPU • Serial number (first five digits) of "10012" or later when used with the Q03UDECPU, Q04UDEHCPU, Q06UDEHCPU, Q13UD(E)HCPU, or Q26UD(E)HCPU • Serial number (first five digits) of "10102" or later when used with the Q10UD(E)HCPU, Q20UD(E)HCPU, Q50UDEHCPU, or Q100UDEHCPU • Cannot be used with the QnUDVCPU and QnUDPVCPU.
		Q12DCCPU-V	• Serial number (first five digits) of "14122" or later when used with the QnUDVCPU • Serial number (first five digits) of "15102" or later and must be in extended mode when used with the QnUDPVCPU
		Q24DHCCPU-V	• Serial number (first five digits) of "14122" or later when used with the QnUDVCPU • Serial number (first five digits) of "15051" or later when used with the QnUDPVCPU
		Q24DHCCPU-VG, Q24DHCCPU-LS, Q26DHCCPU-LS	No function version restriction

Item	Description		
Applicable CPU module[*1]	PC CPU module	PPC-CPU852(MS)-512	• Driver S/W (PPC-DRV-02) version 1.03 or later when used with the Q00UCPU or Q01UCPU • Driver S/W (PPC-DRV-02) version 1.01 or later when used with the Q02UCPU • Driver S/W (PPC-DRV-02) version 1.01 or later when used with the Q03UDCPU, Q04UDHCPU, or Q06UDHCPU • Driver S/W (PPC-DRV-02) version 1.02 or later when used with the Q03UDECPU, Q04UDEHCPU, Q06UDEHCPU, Q13UD(E)HCPU, or Q26UD(E)HCPU • Driver S/W (PPC-DRV-02) version 1.03 or later when used with the Q10UDEHCPU, Q20UDEHCPU, Q50UDEHCPU, or Q100UDEHCPU • Cannot be used with the QnUDVCPU and QnUDPVCPU.
Maximum number of extension base units	7 extension base units, when the Q00UCPU, Q01UCPU, or Q02UCPU is used: 4 extension base units		
Maximum number of mountable I/O modules	65 - (Number of CPU modules), when the Q00UCPU or Q01UCPU is used: 25 - (Number of CPU modules), when the Q02UCPU is used: 37 - (Number of CPU modules)		
Applicable main base unit	Q33B, Q35B, Q38B, Q312B		
Applicable extension base unit	Type requiring no power supply module (Q series)	Q52B, Q55B	
	Type requiring power supply module (Q series)	Q63B, Q65B, Q68B, Q612B	
	Type requiring no power supply module (AnS series)[*3*5]	QA1S51B, QA1S6ADP+A1S5□B[*6]	
	Type requiring power supply module (AnS series)[*3*4]	QA1S65B, QA1S68B, QA1S6ADP+A1S6□B[*6]	
	Type requiring no power supply module (A series)[*3]	QA6ADP+A5□B	
	Type requiring power supply module (A series)[*3]	QA65B, QA68B, QA6ADP+A6□B	
Applicable extension cable	QC05B, QC06B, QC12B, QC30B, QC50B, QC100B		
Applicable power supply module	Power supply module (Q series)	Q61P-A1, Q61P-A2, Q61P, Q62P, Q63P, Q64P, Q64PN	
	Power supply module (AnS series)[*3]	A1S61PN, A1S62PN, A1S63P	
	Power supply module (A series)[*3]	A61P, A61PN, A62P, A63P, A61PEU, A62PEU	

*1 For the CPU modules that can be combined and their mounting positions, refer to Page 63, Section 3.3.2.

*2 When the Q00UCPU, Q01UCPU, or Q02UCPU is used as CPU No.1, two more CPU modules (CPU No.2 and No.3) can be mounted. The following CPU modules can be mounted as CPU No.2 and No.3.

CPU module	Model
Motion CPU	Q172CPUN(-T), Q173CPUN(-T), Q172HCPU(-T), Q173HCPU(-T)
C Controller module	Q06CCPU-V, Q06CCPU-V-B, Q12DCCPU-V, Q24DHCCPU-V, Q24DHCCPU-VG, Q24DHCCPU-LS, Q26DHCCPU-LS
PC CPU module	PPC-CPU852(MS)-512

*3 These modules and units can be used when a Universal model QCPU with a serial number (first five digits) of "13102" or later is set as the control CPU of AnS/A series modules. These modules and units cannot be used in a multiple CPU system containing a Process CPU and a Universal model Process CPU. (☞Page 191, Appendix 3)

*4 When the QA1S6□B is used as an extension base unit, the QA6ADP+A5□B/A6□B cannot be connected.

*5 Since the QA1S51B does not have an extension cable connector (OUT), it cannot be used with the QA6□B or QA6ADP+A5□B/A6□B.

*6 When the QA1S6ADP+A1S5□B/A1S6□B is used, the maximum number of extension base units is 1, and the maximum number of I/O modules that can be mounted is 20 minus the number of CPU modules. When the QA1S6ADP-S1+A1S5□B/A1S6□B is used, the maximum number of extension base units is 3, and the maximum number of I/O modules that can be mounted is 36 minus the number of CPU modules.

(b) Precautions

- If I/O modules are mounted exceeding the maximum number, "SP.UNIT LAY ERR" (error code: 2124) occurs.
- "Number of CPU modules" indicates the number set in "No. of PLC" of PLC parameter ("Multiple CPU Setting").
- When a C Controller module which occupies three slots is used, the maximum number of mountable I/O modules will be two smaller than the number defined in the table on Page 58, Section 3.3.1 (2) (a).
- A PC CPU module occupies two slots. When this module is used, the maximum number of mountable I/O modules will be one smaller than the number defined in the table on Page 58, Section 3.3.1 (2) (a).

(3) When a redundant power main base unit (Q3□RB) is used

(a) Available modules, the number of extension base units, and the number of mountable modules

Item	Description		
Number of CPU modules	4 CPU modules		
Applicable CPU module*1	Universal model QCPU	Q00UCPU, Q01UCPU, Q02UCPU	The modules can be used as CPU No.1.*2
		Q03UD(E)CPU, Q03UDVCPU, Q04UD(E)HCPU, Q04UDVCPU, Q04UDPVCPU, Q06UD(E)HCPU, Q06UDVCPU, Q06UDPVCPU, Q10UD(E)HCPU, Q13UD(E)HCPU, Q13UDVCPU, Q13UDPVCPU, Q20UD(E)HCPU, Q26UD(E)HCPU, Q26UDVCPU, Q26UDPVCPU, Q50UDEHCPU, Q100UDEHCPU	No function version restriction
	High Performance model QCPU	Q02(H)CPU, Q06HCPU, Q12HCPU, Q25HCPU	Function version B
	Process CPU	Q02PHCPU, Q06PHCPU, Q12PHCPU, Q25PHCPU	No function version restriction
	C Controller module	Q24DHCCPU-V	• Serial number (first five digits) of "14122" or later when used with the QnUDVCPU • Serial number (first five digits) of "15051" or later when used with the QnUDPVCPU
		Q24DHCCPU-VG, Q24DHCCPU-LS, Q26DHCCPU-LS	No function version restriction
Maximum number of extension base units	7 extension base units (when the Q00UCPU, Q01UCPU, or Q02UCPU is used: 4 extension base units)		
Maximum number of mountable I/O modules	65 - (Number of CPU modules) when the Q00UCPU or Q01UCPU is used: 25 - (Number of CPU modules), when the Q02UCPU is used: 37 - (Number of CPU modules)		
Applicable main base unit	Q38RB		
Applicable extension base unit	Type requiring no power supply module (Q series)	Q52B, Q55B	
	Redundant power extension base unit	Q68RB	
Applicable extension cable	QC05B, QC06B, QC12B, QC30B, QC50B, QC100B		
Applicable power supply module	Q63RP, Q64RP (The Q63RP and Q64RP can be mounted on the same redundant power supply base unit.)		

*1 For the CPU modules that can be combined and their mounting positions, refer to Page 63, Section 3.3.2.

*2 When the Q00UCPU, Q01UCPU, or Q02UCPU is used as CPU No.1, one more CPU module (CPU No.2) can be mounted. The following CPU modules can be mounted as CPU No.2.

CPU module	Model
C Controller module	Q24DHCCPU-V, Q24DHCCPU-VG, Q24DHCCPU-LS, Q26DHCCPU-LS

(b) Precautions

- If I/O modules are mounted exceeding the maximum number, "SP.UNIT LAY ERR" (error code: 2124) occurs.
- "Number of CPU modules" indicates the number set in "No. of PLC" of PLC parameter ("Multiple CPU Setting").
- When a C Controller module which occupies three slots is used, the maximum number of mountable I/O modules will be two smaller than the number defined in the table on Page 61, Section 3.3.1 (3) (a).

(4) When a slim type main base unit (Q3□SB) is used

(a) Available modules, the number of extension base units, and the number of mountable modules

Item	Description		
Number of CPU modules	3 CPU modules		
Applicable CPU module*1	Universal model QCPU	Q00UCPU, Q01UCPU, Q02UCPU	The modules can be used as CPU No.1.*2
		Q03UD(E)CPU, Q03UDVCPU, Q04UD(E)HCPU, Q04UDVCPU, Q06UD(E)HCPU, Q06UDVCPU, Q10UD(E)HCPU, Q13UD(E)HCPU, Q13UDVCPU, Q20UD(E)HCPU, Q26UD(E)HCPU, Q26UDVCPU, Q50UDEHCPU, Q100UDEHCPU	No function version restriction
	High Performance model QCPU	Q02(H)CPU, Q06HCPU, Q12HCPU, Q25HCPU	Function version B
	C Controller module	Q06CCPU-V, Q06CCPU-V-B	• Serial number (first five digits) of "10102" or later when used with the Q00UCPU, Q01UCPU, or Q02UCPU • Serial number (first five digits) of "10012" or later when used with the Q03UDECPU, Q04UDEHCPU, Q06UDEHCPU, Q13UD(E)HCPU, or Q26UD(E)HCPU • Serial number (first five digits) of "10102" or later when used with the Q00UCPU, Q01UCPU, Q02UCPU, Q10UD(E)HCPU, Q20UD(E)HCPU, Q50UDEHCPU, or Q100UDEHCPU • Cannot be used with the QnUDVCPU.
		Q12DCCPU-V	Serial number (first five digits) of "14122" or later when used with the QnUDVCPU
Maximum number of extension base units	Extension not allowed		
Maximum number of mountable I/O modules	Q32SB	3 - (Number of CPU modules)	
	Q33SB	4 - (Number of CPU modules)	
	Q35SB	6 - (Number of CPU modules)	
Applicable extension cable	Q32SB, Q33SB, Q35SB		
Applicable power supply module	Q61SP		

*1 For the CPU modules that can be combined and their mounting positions, refer to Page 63, Section 3.3.2.

*2 When the Q00UCPU, Q01UCPU, or Q02UCPU is used as CPU No.1, one more CPU module (CPU No.2) can be mounted. The following CPU modules can be mounted as CPU No.2.

CPU module	Model
C Controller module	Q06CCPU-V, Q06CCPU-V-B, Q12DCCPU-V

(b) Precautions

- Slim type main base units do not have an extension cable connector. Therefore, no extension base unit or GOT can be bus-connected.
- Four CPU modules cannot be mounted because the power consumption of the CPU modules exceeds the rated output current of the power supply module (Q61SP).
- "Number of CPU modules" indicates the number set in "No. of PLC" of PLC parameter ("Multiple CPU Setting").

3.3.2 CPU module combinations and mounting positions

This section describes the combinations and mounting positions of CPU modules when a Universal model QCPU is used as CPU No.1.

Note that the CPU modules that can be mounted differ depending on the main base unit used. (☞Page 55, Section 3.3.1)

(1) Combinations

CPU No.1	Number of CPU modules that can be mounted as CPU No.2 or others							Maximum number of mountable modules (including CPU No.1)
	High Performance model QCPU, Process CPU, Universal model QCPU*2*5*6	Motion CPU		C Controller module*1*5		PC CPU module*1*6		
		Q172CPUN(-T), Q173CPUN(-T), Q172HCPU(-T), Q173HCPU(-T)*3	Q172DCPU(-S1), Q173DCPU(-S1), Q172DSCPU, Q173DSCPU*4	Q06CCPU-V, Q06CCPU-V-B, Q12DCCPU-V	Q24DHC CPU-V, Q24DHC CPU-VG, Q24DHC CPU-LS, Q26DHC CPU-LS	PPC-CPU686 (MS)-64, PPC-CPU686 (MS)-128	PPC-CPU852 (MS)-512	
Q00UCPU, Q01UCPU, Q02UCPU	Cannot be used together.	0 to 1	Cannot be used together.	0 to 1	0 to 1	Cannot be used together.	0 to 1	3
Universal model QCPU other than the above	0 to 3	Cannot be used together.	0 to 3	0 to 3	0 to 1	Cannot be used together.	0 to 1	4

*1 A C Controller module and a PC CPU module cannot be mounted on the same main base unit.

*2 The Q00UCPU, Q01UCPU, and Q02UCPU can be used only as CPU No.1.

*3 The module and a C Controller module (Q12DCCPU-V, Q24DHCCPU-V, Q24DHCCPU-VG, Q24DHCCPU-LS, Q26DHCCPU-LS) cannot be mounted on the same main base unit.

*4 When the Q172DCPU(-S1), Q173DCPU(-S1), Q172DSCPU, or Q173DSCPU is used, only the following CPU modules can be mounted on the same main base unit.
- Universal model QCPU (except the Q00UCPU, Q01UCPU, and Q02UCPU)
- C Controller module (Q12DCCPU-V, Q24DHCCPU-V, Q24DHCCPU-VG, Q24DHCCPU-LS, Q26DHCCPU-LS)

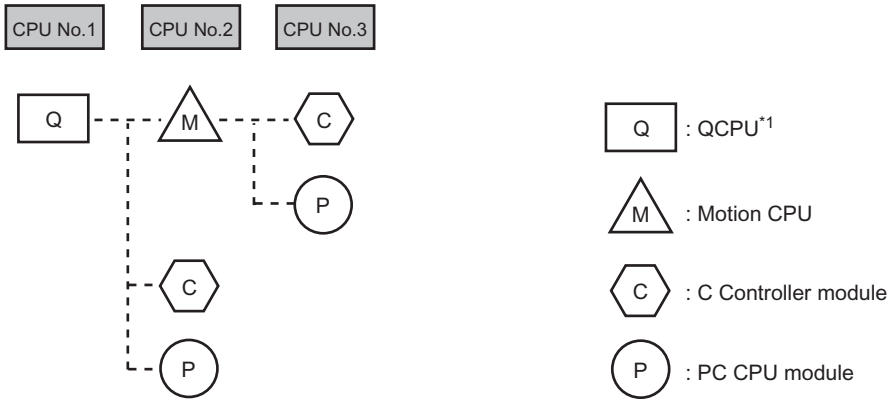
*5 A QnUDVCPU, a QnUDPVCPU, and a C Controller module (Q06CCPU-V or Q06CCPU-V-B) cannot be mounted on the same main base unit.
Also, a QnUDPVCPU and a C Controller module (Q12DCCPU-V) cannot be mounted on the same main base unit.

*6 A QnUDVCPU, a QnUDPVCPU, and a PC CPU module cannot be mounted on the same main base unit.

(2) Mounting positions

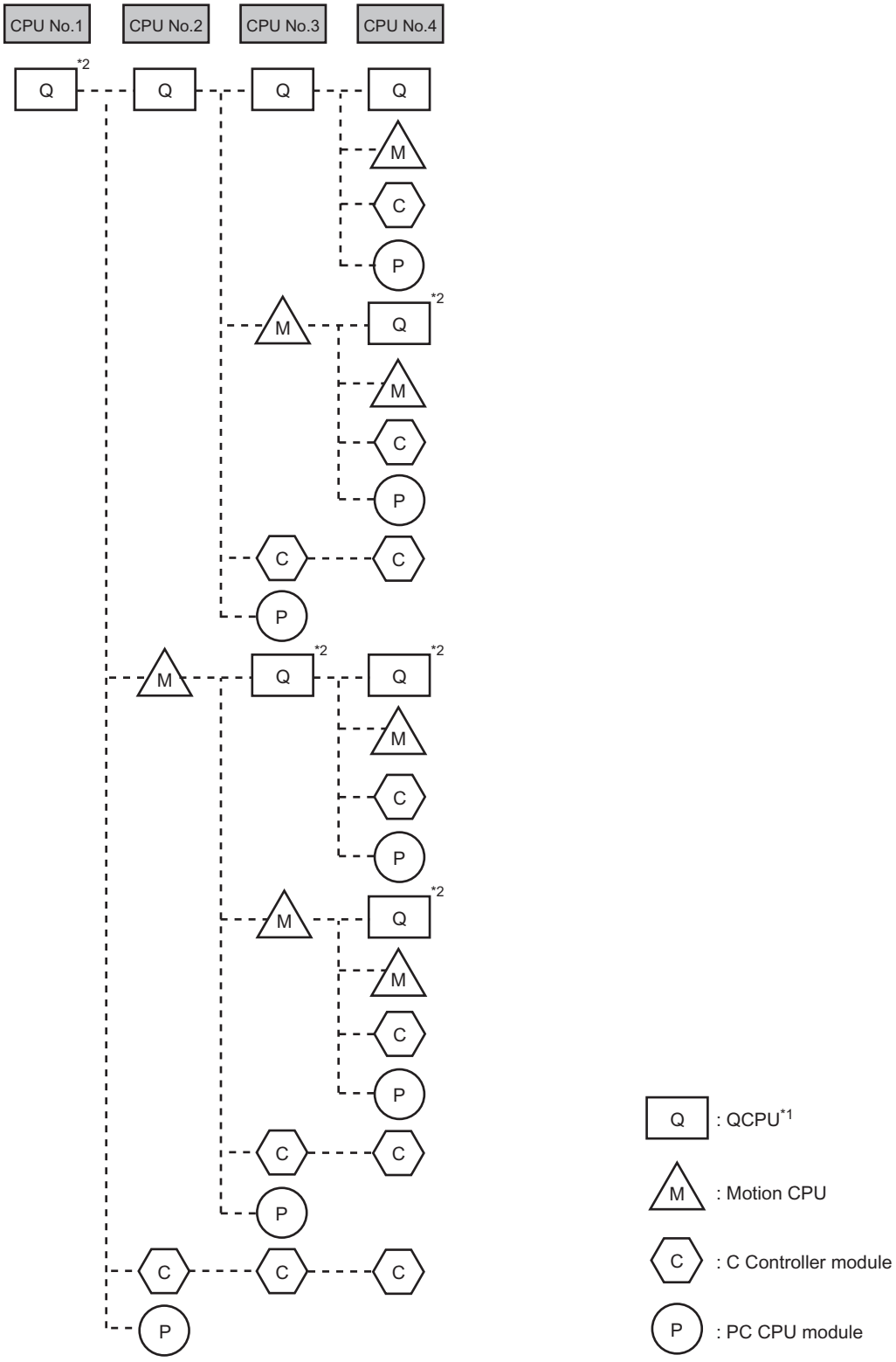
The following shows the possible combinations of mounting positions of CPU modules in a multiple CPU system.

- When the Q00UCPU, Q01UCPU, or Q02UCPU is used as CPU No.1



*1 The QCPU indicates the Q00UCPU, Q01UCPU, or Q02UCPU.

• When a CPU module other than the Q00UCPU, Q01UCPU, or Q02UCPU is used as CPU No.1



*1 The QCPU used as CPU No.1 indicates a Universal model QCPU (except the Q00UCPU, Q01UCPU, and Q02UCPU). The QCPU used as CPU No.2 or later indicates a High Performance model QCPU, Process CPU, or Universal model QCPU (except the Q00UCPU, Q01UCPU, and Q02UCPU).

*2 The QCPU indicates a Universal model QCPU (except the Q00UCPU, Q01UCPU, and Q02UCPU).

(a) Universal model QCPU

Only one Q00UCPU, Q01UCPU, or Q02UCPU can be mounted in the CPU slot (the slot on the right of the power supply module).

Up to four Universal model QCPUs other than the Q00UCPU, Q01UCPU, and Q02UCPU can be mounted in the CPU slot (the slot on the right of the power supply module) to slot 2 of the main base unit.

(b) High Performance model QCPU or Process CPU

When the Q00UCPU, Q01UCPU, or Q02UCPU is used, no High Performance model QCPU or Process CPU can be mounted.

When a Universal model QCPU other than the Q00UCPU, Q01UCPU, and Q02UCPU is used, up to three High Performance QCPUs and/or Process CPUs can be mounted in slot 0 to slot 2 of the main base unit.

(c) Motion CPU

When the Q00UCPU, Q01UCPU, or Q02UCPU is used, only one Motion CPU can be mounted in slot 0 of the main base unit.

When a Universal model QCPU other than the Q00UCPU, Q01UCPU, and Q02UCPU is used, up to three Motion CPUs can be mounted in slot 0 to slot 2.

Only a Universal model QCPU, Motion CPU, C Controller module, or PC CPU module can be mounted on the right of the Motion CPU.

(d) C Controller module

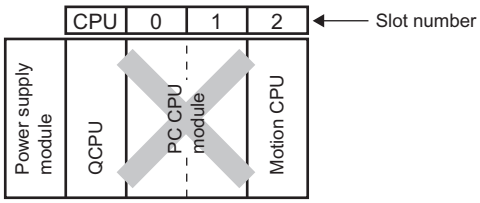
When the Q00UCPU, Q01UCPU, or Q02UCPU is used, only one C Controller module can be mounted on the rightmost slot available for CPU modules.

When a Universal model QCPU other than the Q00UCPU, Q01UCPU, and Q02UCPU is used, up to three C Controller modules can be mounted on the right of the following CPU modules. For a C Controller module which occupies three slots, only one module can be mounted.

- High Performance model QCPU
- Process CPU
- Universal model QCPU (except the Q00UCPU, Q01UCPU, and Q02UCPU)
- C Controller module
- Motion CPU (Q172DCPU(-S1), Q173DCPU(-S1), Q172DSCPU, or Q173DSCPU)

(e) PC CPU module

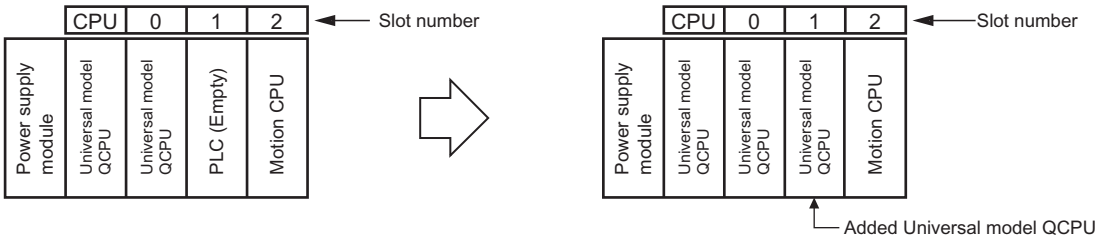
Only one PC CPU module can be mounted on the rightmost slot available for CPU modules. No CPU module can be mounted on the right of the PC CPU module.



(f) Empty slot setting

Empty slots can be reserved for future addition of CPU modules. Set the number of CPU modules including empty slots in "No. of PLC" of PLC parameter ("Multiple CPU Setting"). Then, set "PLC (Empty)" to the type of a target slot in PLC parameter ("I/O Assignment").

Ex. Setting "PLC (Empty)" between CPU modules



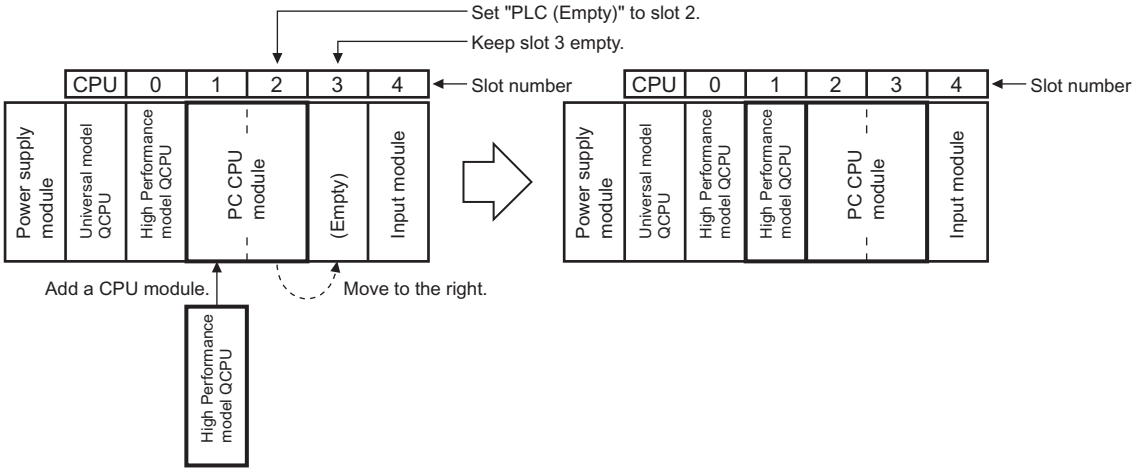
Point

When a Universal model QCPU is used, "PLC (Empty)" can be set between CPU modules.
This is useful when adding a CPU module to the system in the future. No program modification is required because the CPU number set as an empty slot can be assigned to the added CPU module.

Note, however, that when the following CPU module is used, "PLC (Empty)" cannot be set to the left of the CPU module.

- High Performance model QCPU
- Process CPU

To add a High Performance mode QCPU to the system where a C Controller module or PC CPU module is used, move the C Controller module or PC CPU module to the right to allow addition of a CPU module.



3.3.3 Available I/O modules and intelligent function modules

Refer to the system configuration using a a High Performance model QCPU or Process CPU as CPU No.1.
(☞Page 53, Section 3.2.3)

3.4 Applicable Software

This section describes software packages applicable in a multiple CPU system.

(1) Applicable GX Works2, GX Developer, and PX Developer

The following table lists the applicable versions of GX Works2, GX Developer, and PX Developer.

QCPU		Version		
		GX Works2	GX Developer	PX Developer
Basic model QCPU		1.15R or later	8.00A or later	Use prohibited
High Performance model QCPU			6.00A or later	
Process CPU	Q02PHCPU, Q06PHCPU	1.87R or later	8.68W or later	1.18U or later*1
	Q12PHCPU, Q25PHCPU		7.10L or later	1.00A or later*1*2
Universal model QCPU	Q00UCPU, Q01UCPU	1.15R or later	8.76E or later	Use prohibited
	Q02UCPU, Q03UDCPU, Q04UDHCPU, Q06UDHCPU		8.48A or later	Use prohibited
	Q10UDHCPU, Q20UDHCPU		8.76E or later	Use prohibited
	Q13UDHCPU, Q26UDHCPU		8.62Q or later	Use prohibited
	Q03UDVCPU, Q04UDVCPU, Q06UDVCPU, Q13UDVCPU, Q26UDVCPU	1.98C or later	Use prohibited	Use prohibited
	Q04UDPVCPU, Q06UDPVCPU, Q13UDPVCPU, Q26UDPVCPU	1.492N or later	Use prohibited	1.38Q or later
	Q03UDECPU, Q04UDEHCPU, Q06UDEHCPU, Q13UDEHCPU, Q26UDEHCPU	1.15R or later	8.68W or later	Use prohibited
	Q10UDEHCPU, Q20UDEHCPU		8.76E or later	Use prohibited
	Q50UDEHCPU, Q100UDEHCPU	1.31H or later	Use prohibited	Use prohibited

*1 To use GX Works2 in combination with PX Developer, use GX Works2 version 1.98C or later.

*2 To use GX Developer in combination with PX Developer, use GX Developer version 7.12N or later.

(2) Applicable GX Configurator

The following tables list the applicable versions of GX Configurator. Applicable GX Configurator versions differ depending on the intelligent function module used. (Manual for the intelligent function module used)

(a) When a Basic model QCPU, High Performance model QCPU, or Process CPU is used

Product	Version		
	Basic model QCPU	High Performance model QCPU	Process CPU
GX Configurator-AD	1.10L or later	SW0D5C-QADU 20C or later	1.13P or later
GX Configurator-DA		SW0D5C-QDAU 20C or later	
GX Configurator-SC		SW0D5C-QSCU 20C or later	
GX Configurator-CT		SW0D5C-QCTU 20C or later	
GX Configurator-TI		1.00A or later	
GX Configurator-TC		SW0D5C-QCTU 00A or later	
GX Configurator-FL		SW0D5C-QFLU 00A or later	
GX Configurator-QP	2.10L or later	2.00A or later	2.13P or later
GX Configurator-PT	1.10L or later	1.00A or later	1.13P or later
GX Configurator-MB	1.00A or later	1.00A or later	1.00A or later
GX Configurator-AS	1.13P or later	1.13P or later	1.13P or later
GX Configurator-DN	1.10L or later	1.00A or later	1.13P or later
GX Configurator-DP	7.00A or later	7.00A or later	7.00A or later*1

*1 To use GX Configurator with the Q02PH/Q06PHCPU, use the version 7.04E or later.

(b) When a Universal model QCPU is used

Product	Version compatible with the Universal model QCPU			
	Used with Q02U/Q03UD/Q04UDH/ Q06UDHCPU	Used with Q13UDH/Q26UDHCPU	Used with Q03UDE/Q04UDEH/ Q06UDEH/Q13UDEH/ Q26UDEHCPU	Used with Q00U/Q01U/Q10UDH/ Q20UDH/Q10UDEH/ Q20UDEHCPU
GX Configurator-AD	2.05F or later*1	2.05F or later*2	2.05F or later*3	2.05F or later*4
GX Configurator-DA	2.06G or later*1	2.06G or later*2	2.06G or later*3	2.06G or later*4
GX Configurator-SC	2.12N or later*1	2.12N or later*2	2.17T or later*3	2.17T or later*4
GX Configurator-CT	1.25AB or later*1	1.25AB or later*2	1.25AB or later*3	1.25AB or later*4
GX Configurator-TI	1.24AA or later*1	1.24AA or later*2	1.24AA or later*3	1.24AA or later*4
GX Configurator-TC	1.23Z or later*1	1.23Z or later*2	1.23Z or later*3	1.23Z or later*4
GX Configurator-FL	1.23Z or later*1	1.23Z or later*2	1.23Z or later*3	1.23Z or later*4
GX Configurator-QP	2.25B or later	2.29F or later	2.30G or later*5	2.32J or later
GX Configurator-PT	1.23Z or later*1	1.23Z or later*2	1.23Z or later*3	1.23Z or later*4
GX Configurator-MB	1.08J or later*1	1.08J or later*2	1.08J or later*3	1.08J or later*4
GX Configurator-AS	1.21X or later*1	1.21X or later*2	1.21X or later*3	1.21X or later*4
GX Configurator-DN	1.23Z or later*1	1.23Z or later*2	1.24AA or later*3	1.24AA or later*4
GX Configurator-DP*6	7.02C or later*7	7.03D or later	7.03D or later	7.04E or later

*1 The software can be used by installing GX Developer version 8.48A or later.
*2 The software can be used by installing GX Developer version 8.62Q or later.
*3 The software can be used by installing GX Developer version 8.68W or later.
*4 The software can be used by installing GX Developer version 8.76E or later.
*5 GX Configurator-QP version 2.29F can also be used when connected via USB.
*6 To use GX Configurator with the Q50UDEH/Q100UDEHCPU, use the version 7.07H or later.
*7 To use GX Configurator with the Q02UCPU, use the version 7.03D or later.

3.5 Precautions for System Configuration

This section describes restrictions and precautions on system configuration.

(1) Number of mountable modules

The number of mountable modules and supported functions are restricted depending on the CPU module used. For the number of modules that can be connected to each Motion CPU, C Controller module, or PC CPU module, refer to the manual for the CPU module used.

(a) When a Basic model QCPU is used

Product	Model	Maximum number of modules/units per system	
CC-Link IE Controller Network module	• QJ71GP21-SX • QJ71GP21S-SX	Up to 4 modules (One Q00CPU or Q01CPU can control only one module.)	Up to 4 modules in total
MELSECNET/H module	• QJ71LP21 • QJ71BR11 • QJ71LP21-25 • QJ71LP21S-25 • QJ71LP21G • QJ71LP21GE • QJ71NT11B	Up to 4 modules (One Q00CPU or Q01CPU can control only one module on the PLC to PLC network.)	
Ethernet interface module	• QJ71E71 • QJ71E71-B2 • QJ71E71-B5 • QJ71E71-100	Only 1 module (Controlled only by the QCPUs)	
CC-Link system master/local module	• QJ61BT11 • QJ61BT11N	Up to 10 modules*1 (One QCPU can control only two modules.)	
Interrupt module	• QI60	Up to 3 modules*2 (One QCPU can control only one module.)	
High-speed input module (Interrupt module)*4	• QX40H • QX70H • QX80H • QX90H		
High speed data logger module	• QD81DL96	Only 1 module (Controlled by QCPUs or C Controller modules)	
High speed data communication module	• QJ71DC96	Only 1 module (Controlled by QCPUs or C Controller modules)	
GOT	• GOT-A900 series (Bus connection only)*3 • GOT1000 series (Bus connection only)*3	Up to 5 units	

*1 Modules of function version B or later can be mounted.

*2 The number indicates interrupt modules with no interrupt pointer setting. With interrupt pointer setting, no restriction applies.

*3 For the applicable GOT models, refer to the connection manual for the GOT used.

*4 The number of mountable modules is restricted when a high-speed input module is used as an interrupt module by turning off the function switch (SW2).

(b) When a High Performance model QCPU or Process CPU is used

Product	Model	Maximum number of modules/units per system	
CC-Link IE Controller Network module[*4]	• QJ71GP21-SX • QJ71GP21S-SX	Up to 2 modules	Up to 4 modules in total
MELSECNET/H module	• QJ71LP21 • QJ71BR11 • QJ71LP21-25 • QJ71LP21S-25 • QJ71LP21G • QJ71LP21GE • QJ71NT11B	Up to 4 modules	
Ethernet interface module	• QJ71E71 • QJ71E71-B2 • QJ71E71-B5 • QJ71E71-100	Up to 4 modules	
CC-Link system master/local module	• QJ61BT11 • QJ61BT11N	No restriction[*1]	
AnS series special function module[*2]	• A1SJ71PT32-S3 • A1SJ71T32-S3	No restriction (Auto refresh setting not allowed)	
	• A1SD51S • A1SD21-S1 • A1SJ71J92-S3 (When using GET/PUT service) • A1SJ71AP23Q • A1SJ71AR23Q • A1SJ71AT23BQ	Up to 6 modules in total	
Interrupt module	• A1SI61[*2]	Only 1 module	
	• QI60	Up to 4 modules (Up to 3 modules when A1SI61 is used. A QCPU can control only 1 module.)	
High-speed input module (Interrupt module)[*5]	• QX40H • QX70H • QX80H • QX90H		
High speed data logger module	• QD81DL96	Up to 4 modules (Controlled by QCPUs or C Controller modules. A QCPU or C Controller module can control only 1 module.)	
High speed data communication module	• QJ71DC96	Up to 4 modules (Controlled by QCPUs or C Controller modules. A QCPU or C Controller module can control only 1 module.)	
GOT	• GOT-A900 Series (Bus connection only)[*3] • GOT1000 Series (Bus connection only)[*3]	Up to 5 units	

*1 One CPU module can control the following number of modules by setting CC-Link network parameters.
• CPU module with a serial number (first five digits) of "08031" or earlier: Up to 4 modules
• CPU module with a serial number (first five digits) of "08032" or later: Up to 8 modules
There is no restriction on the number of mounted modules when the parameters are set with the CC-Link dedicated instructions.

*2 The module can be used only when a High Performance model QCPU is set to a control module. However, it cannot be used if a Process CPU is used in combination. (Page 191, Appendix 3)

*3 For the applicable GOT models, refer to the connection manual for the GOT used.

*4 The module can be used with the following CPU modules.
• High Performance model QCPU with a serial number (first five digits) of "09012" or later
• Process CPU with a serial number (first five digits) of "10042" or later

*5 The number of mountable modules is restricted when a high-speed input module is used as an interrupt module by turning off the function switch (SW2).

Remark

For the restrictions on mounting A-series modules on the QA6□B or QA6ADP+A5□B/A6□B, refer to the following.

QA65B/QA68B Extension Base Unit User's Manual

QA6ADP QA Conversion Adapter Module User's Manual

For the restrictions on mounting AnS-series modules on the QA1S6ADP+A1S5□B/A1S6□B, refer to the following.

QA1S6ADP Q-AnS Base Unit Conversion Adapter User's Manual

QA1S6ADP-S1 Q-AnS Base Unit Conversion Adapter User's Manual

(c) When a Universal model QCPU is used

Product	Model	Maximum number of modules/units per system
CC-Link IE Controller Network module[*4]	• QJ71GP21-SX • QJ71GP21S-SX	Up to 4 modules in total
MELSECNET/H module	• QJ71LP21 • QJ71BR11 • QJ71LP21-25 • QJ71LP21S-25 • QJ71LP21G • QJ71LP21GE • QJ71NT11B	With the Q00UCPU, Q01UCPU, or Q02UCPU, the maximum number of connectable modules is as follows: • Q02UCPU: Up to 2 modules in total • Q00UCPU or Q01UCPU: Only 1 module
CC-Link IE Field Network module	• QJ71GF11-T2	No restriction[*6]
Ethernet interface module	• QJ71E71 • QJ71E71-B2 • QJ71E71-B5 • QJ71E71-100	Up to 4 modules With the Q00UCPU, Q01UCPU, or Q02UCPU, the maximum number of connectable modules is as follows: • Q02UCPU: Up to 2 modules • Q00UCPU or Q01UCPU: Only 1 module
CC-Link system master/local module	• QJ61BT11 • QJ61BT11N	No restriction[*1*5]
AnS series special function module[*8]	• A1SJ71PT32-S3 • A1SJ71T32-S3	No restriction (Auto refresh setting not allowed)
	• A1SD51S • A1SD21-S1 • A1SJ71J92-S3 (When using GET/PUT service) • A1SJ71AP23Q • A1SJ71AR23Q • A1SJ71AT23BQ	Up to 6 modules in total
Interrupt module	• A1SI61[*8]	Only 1 module
	• QI60	Up to 4 modules[*3]
High-speed input module (Interrupt module)[*7]	• QX40H • QX70H • QX80H • QX90H	
High speed data logger module[*9]	• QD81DL96	Up to 4 modules (Controlled by QCPUs or C Controller modules. A QCPU or C Controller module can control only 1 module.)
High speed data communication module	• QJ71DC96	Up to 4 modules (Controlled by QCPUs or C Controller modules. A QCPU or C Controller module can control only 1 module.)
GOT	• GOT1000 Series (for bus connection only)[*2]	Up to 5 units

*1 One CPU module can control the following number of modules by setting CC-Link network parameters.
• Q00UCPU or Q01UCPU: Up to 2 modules
• Q02UCPU: Up to 4 modules
• Other CPU modules: Up to 8 modules
There is no restriction on the number of mounted modules when the parameters are set with the CC-Link dedicated instructions.

*2 For the applicable GOT models, refer to the connection manual for the GOT used.

*3 The number indicates interrupt modules with no interrupt pointer setting. With interrupt pointer setting, no restriction applies.

*4 When one of the following CPU modules is used in the multiple CPU system, the number of modules can be mounted is restricted to two.
• High Performance model QCPU
• Process CPU

*5 Modules of function version B or later can be mounted.

*6 One CPU module can control the following number of modules by setting CC-Link IE Field Network parameters using a programming tool.
• Q00UCPU or Q01UCPU: Up to 2 modules
• Q02UCPU: Up to 4 modules
• Other CPU modules: Up to 8 modules
There is no restriction on the number of mounted modules when the parameters are set with the CC-Link IE Field Network dedicated instructions.

*7 The number of mountable modules is restricted when a high-speed input module is used as an interrupt module by turning off the function switch (SW2).

*8 The module can be used when a Universal model QCPU with a serial number (first five digits) of "13102" or later is set to a control module. However, it cannot be used with a Process CPU and a Universal model Process CPU. (☞ Page 191, Appendix 3)

*9 With a High-speed Universal model QCPU and a Universal model Process CPU, only high speed data logger modules with a serial number (first five digits) of "14122" or later can be used.

Remark

For the restrictions on mounting A-series modules on the QA6□B or QA6ADP+A5□B/A6□B, refer to the following.

QA65B/QA68B Extension Base Unit User's Manual
QA6ADP QA Conversion Adapter Module User's Manual

For the restrictions on mounting AnS-series modules on the QA1S6ADP+A1S5□B/A1S6□B, refer to the following.

QA1S6ADP Q-AnS Base Unit Conversion Adapter User's Manual
QA1S6ADP-S1 Q-AnS Base Unit Conversion Adapter User's Manual

(2) Modules that have restrictions when used with an Universal model QCPU

For modules that have restrictions when used with an Universal model QCPU, refer to the following manual.

QnUCPU User's Manual (Function Explanation, Program Fundamentals)

(3) Combinations of power supply modules, base units, and QCPUs

There are some restrictions on combinations of power supply modules, base units, and QCPUs. (QCPU User's Manual (Hardware Design, Maintenance and Inspection)

Ex. Redundant power supply modules can be mounted only on redundant power main base units or redundant power extension base units.

(4) Precautions for using a QCPU of function version A

If a QCPU of function version A is used in a multiple CPU system, an error occurs. To configure a multiple CPU system with QCPUs, use CPU modules of function version B or later.

CPU No.1	Other than CPU No.1	Error in CPU No.1	Error in other than CPU No.1
QCPU (function version A)	QCPU (function version A)	"UNIT VERIFY ERROR" (error code: 2000)	"SP.UNIT LAY ERROR" (error code: 2125)
QCPU (function version A)	QCPU (function version B)	"UNIT VERIFY ERROR" (error code: 2000)	"MULTI EXE.ERROR" (error code: 7010)
QCPU (function version B)	QCPU (function version A)	"MULTI EXE.ERROR" (error code: 7010)	"SP.UNIT LAY ERROR" (error code: 2125)

(5) Precautions for using the high-speed interrupt function

A High Performance model QCPU, High-speed Universal model QCPU, and Universal model Process CPU support the high-speed interrupt function.

If the parameter with the high-speed interrupt fixed scan interval setting is written, the functions of the CPU module are partly restricted. The restrictions differ depending on the CPU module used. (User's Manual (Function Explanation, Program Fundamentals) for the CPU module used)

Note that the above restrictions do not apply to the High Performance model QCPU with a serial number (first five digits) of "04011" or earlier because the module ignores the high-speed interrupt fixed scan interval setting.

(6) Precautions for using a Motion CPU (Q172DCPU(-S1), Q173DCPU(-S1), Q172DSCPU, or Q173DSCPU)

The Q172DCPU(-S1), Q173DCPU(-S1), Q172DSCPU, or Q173DSCPU can only be mounted on a multiple CPU high-speed main base unit.

Note that do not mount any Motion modules controlled by the Motion CPU in slot 0 to 2 of the multiple CPU high-speed main base unit.

(7) Precautions for connecting a GOT

The following GOT series can be used.

- GOT-A900 series*1
- GOT-F900 series (The Q-mode compatible operating system and communication driver must be installed.)*1
- GOT1000 series

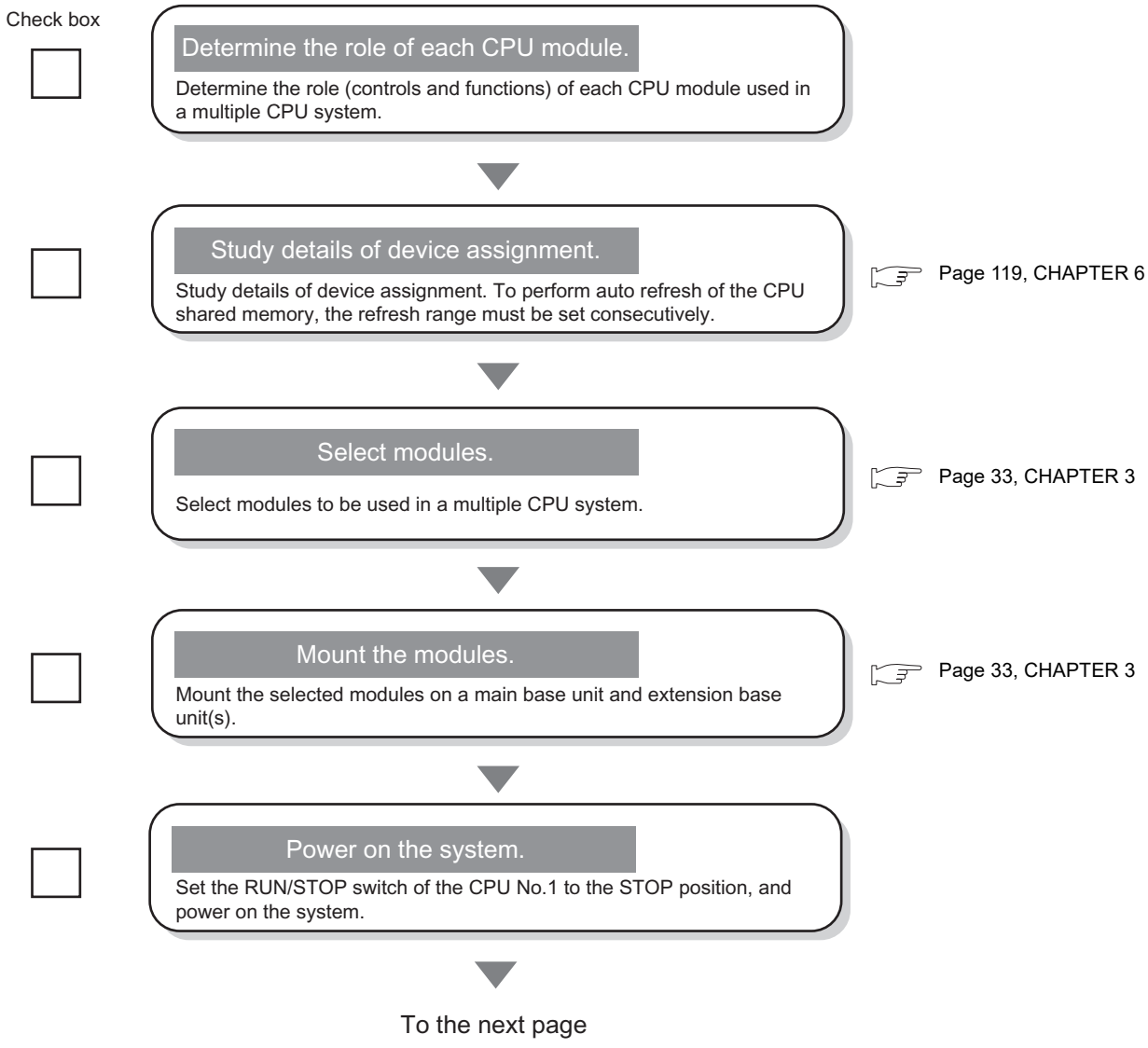
The GOT800 series, A77GOT, and A64GOT cannot be used.

*1 Universal model QCPUs do not support the GOT-A900 and GOT-F900 series.

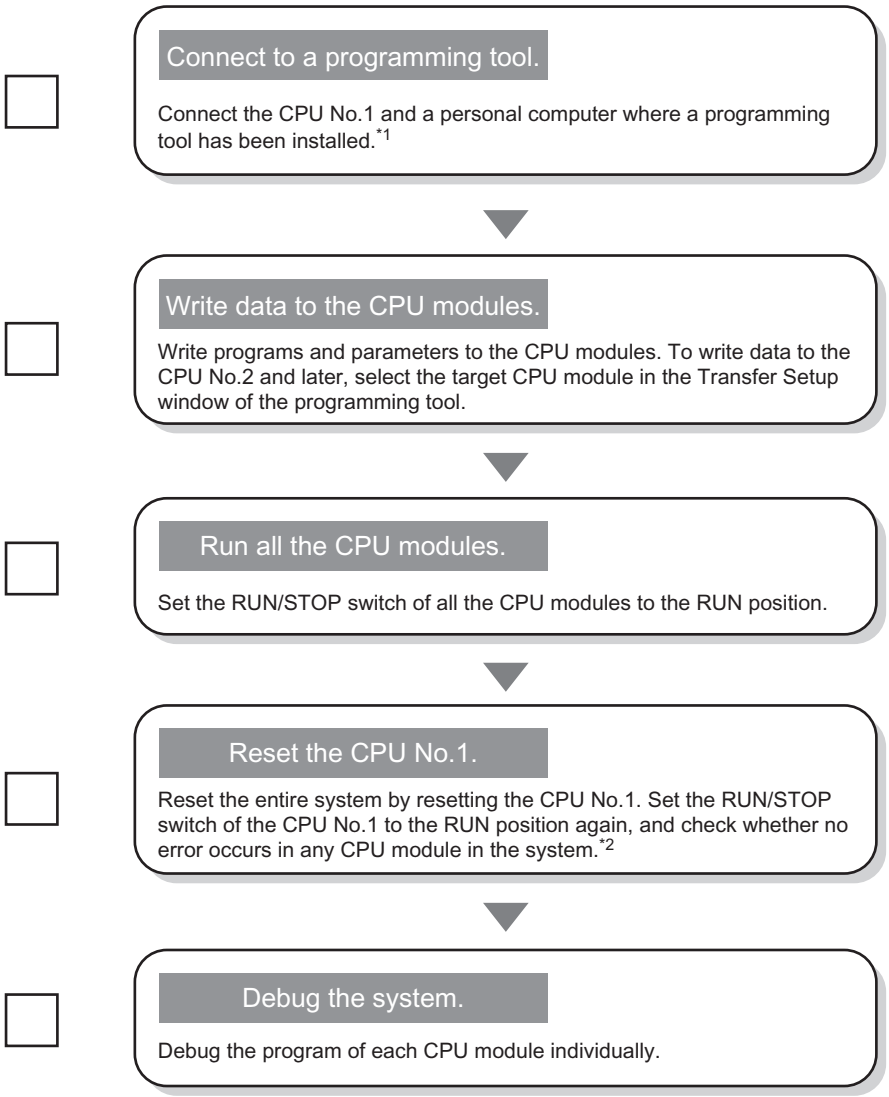
CHAPTER 4 STARTING UP MULTIPLE CPU SYSTEM

This chapter describes the procedure for starting up a multiple CPU system.

4.1 Procedure Before Operation



To the next page



☞ Page 115, Section 5.3

*1 When a PC CPU module is used, the QCPU can be bus-connected to a programming tool by installing the programming tool in the PC CPU module. Select "Q Series Bus" for the "PC side I/F" setting in the "Transfer Setup" window using the programming tool.

*2 If an error has occurred, check the error cause using the programming tool and take corrective action.
An error in the CPU modules can be checked in the "PLC Diagnostics" window.
An error in the I/O modules and intelligent function modules can be checked in the "System Monitor" window.
(QCPU User's Manual (Hardware Design, Maintenance and Inspection))

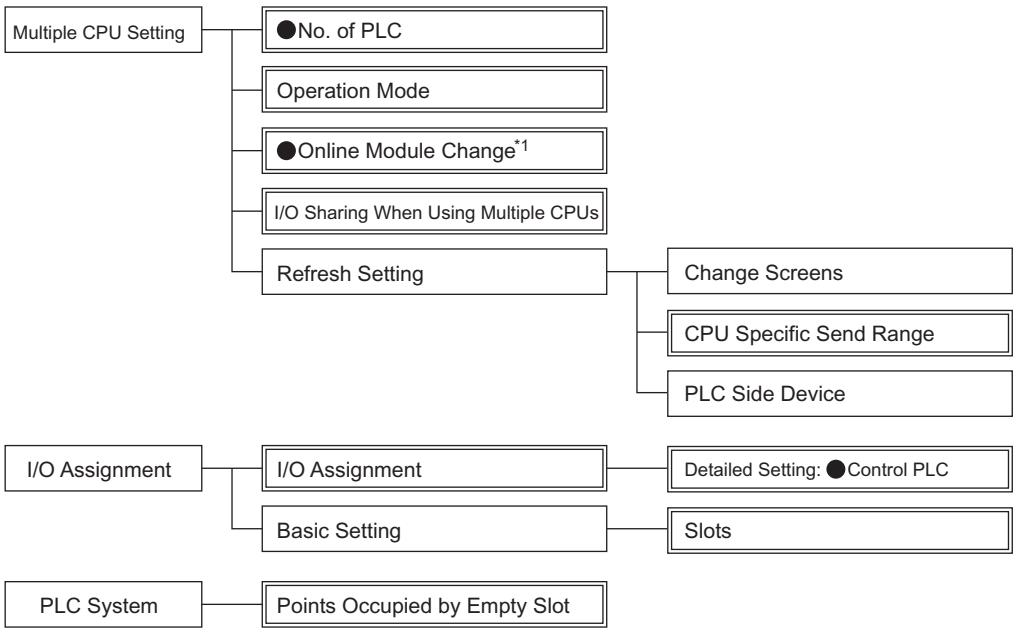
4.2 Operation Settings

This section describes the settings required to operate a multiple CPU system. A system where three Universal model QCPUs are mounted shall be used as an example.

(1) Parameters required

(a) Basic model QCPU, High Performance model QCPU, and Process CPU

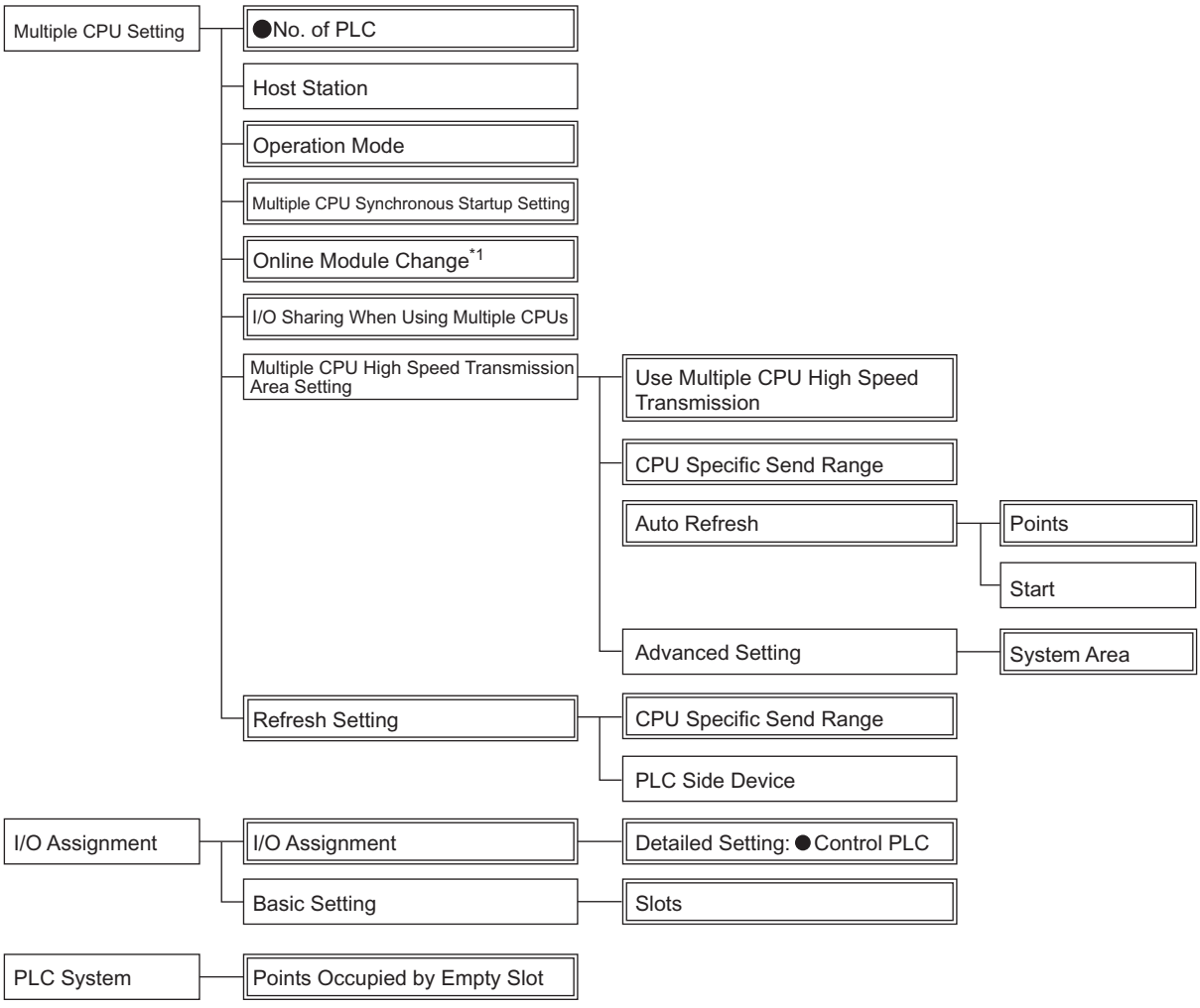
Settings of parameters in double-lined squares, except some parameters, must be the same in all the CPU modules used in a multiple CPU system. (☞ Page 175, Appendix 1.1)



*1 For Basic model QCPUs, the online module change setting is not available.
High Performance model QCPUs do not support the online change function, but the setting is required to replace modules controlled by the Process CPU on the same base unit online.

(b) Universal model QCPU

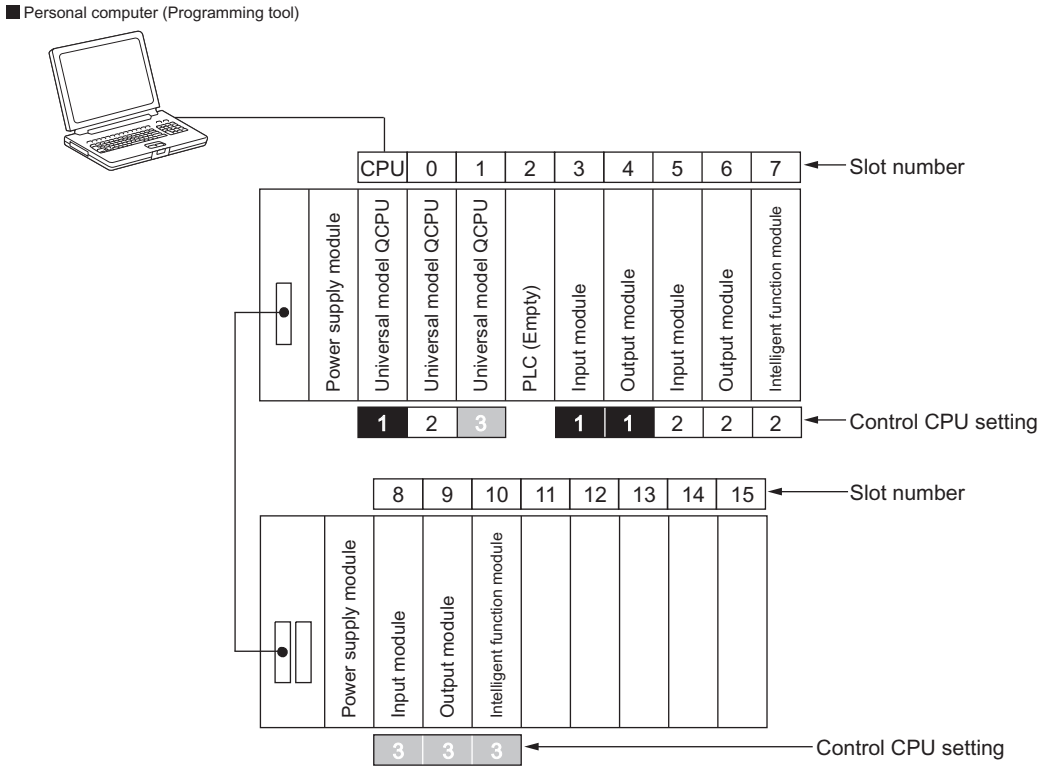
Settings of parameters in double-lined squares, except some parameters, must be the same in all the CPU modules used in a multiple CPU system. (☞ Page 175, Appendix 1.1)



*1 Universal model QCPUs do not support the online change function, but the setting is required to replace modules controlled by the Process CPU on the same base unit online.

4.2.1 System configuration example

This section describes the procedure for setting parameters required in a multiple CPU system, using the following system as an example.



4.2.2 Parameter settings

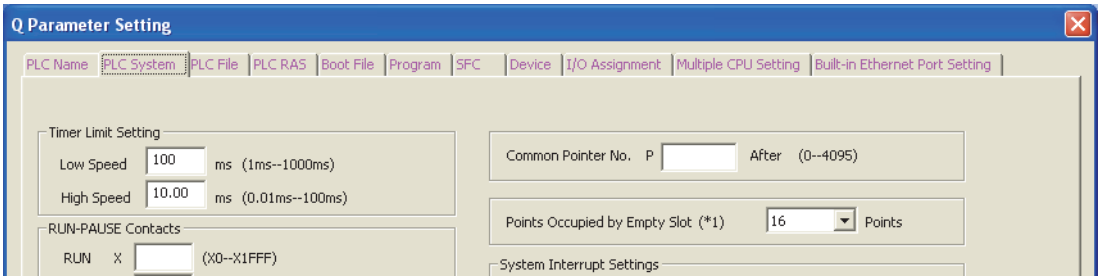
This section describes parameters required for the system configuration on Page 82, Section 4.2.1. Use a programming tool to set parameters.

- Settings of parameters in double-lined squares on Page 80, Section 4.2 (1) must be the same in all the CPU modules in a multiple CPU system.
- The necessity of parameters differs depending on the QCPU used. (☞Page 80, Section 4.2 (1))

(1) Setting parameters (for the first time)

1. Set "Points Occupied by Empty Slot" in the "PLC System" window of PLC parameter.

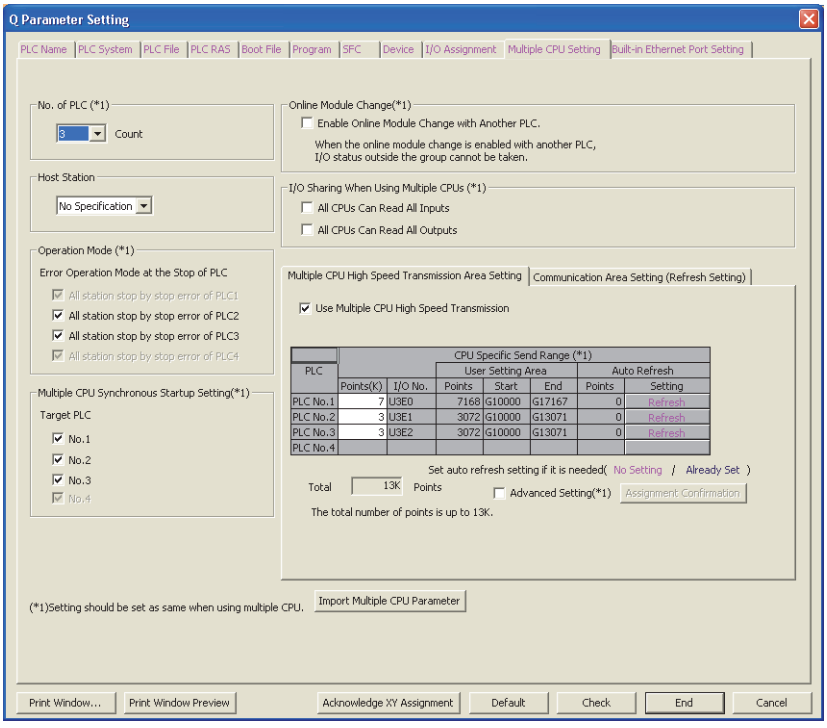
Project window ⇨ [Parameter] ⇨ [PLC Parameter] ⇨ [PLC System] ⇨ "Points Occupied by Empty Slot"

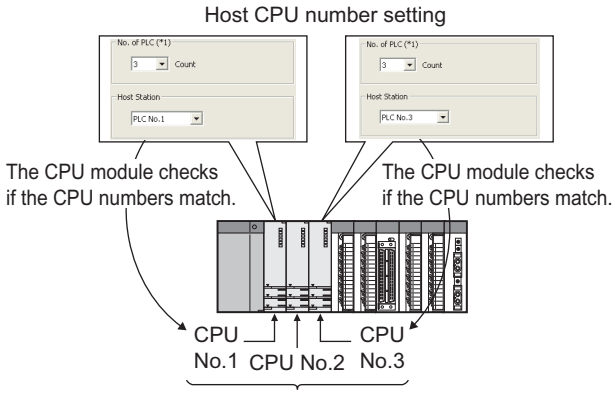


Item	Description	Default
Points Occupied by Empty Slot	Set the number of points occupied by one empty slot.	16 points

2. Set parameters for the multiple CPU system in the "Multiple CPU Setting" window of PLC parameter.

Project window ⇨ [Parameter] ⇨ [PLC Parameter] ⇨ [Multiple CPU Setting]



Item	Description	Default
No. of PLC	Set the number of CPU modules mounted on the main base unit in the multiple CPU system. The number of modules differs depending on the CPU module used as CPU No.1 and the main base unit used. (☞ Page 33, CHAPTER 3) This parameter must be set.	1
Host Station	Set this parameter to check the host CPU number in the multiple CPU system. If this parameter is set, each CPU module checks its own CPU number with the one set in this parameter to see if they match.  CPU numbers are determined by their mounting positions. • When "No Specification" is selected, the host CPU number is not checked. • Host CPU numbers do not need to be set to all the CPU modules in the system. • To set the same "Multiple CPU Setting" parameters to all the CPU modules used in the multiple CPU system, select "No Specification". Parameter settings are shared by all the CPU modules used in the system. The host CPU number can be checked when one of the following CPU modules is used. • Universal model QCPU (except the Q00UCPU, Q01UCPU, and Q02UCPU) • Motion CPU (Q172DCPU(-S1), Q173DCPU(-S1), Q172DSCPU, or Q173DSCPU) • C Controller module (Q12DCCPU-V, Q24DHCCPU-V, Q24DHCCPU-VG, Q24DHCCPU-LS, or Q26DHCCPU-LS)	No Specification
Operation Mode	Select whether to stop or continue the operation of all the CPU modules when a stop error occurs in a CPU module. Set this parameter to continue the operation of other error-free CPU modules if a stop error occurs in a CPU module other than CPU No.1. For example, if the "All station stop by stop error of PLC2" checkbox is unchecked, other CPU modules continue their operation even after a stop error occurs in CPU No.2. The operation mode of CPU No.1 cannot be changed. (☞ Page 105, Section 4.6)	All items selected
Multiple CPU Synchronous Startup Setting	Set this parameter to enable synchronous startup of the CPU modules in the multiple CPU system. (☞ Page 171, Section 6.5) Only Universal model QCPUs support this parameter. Uncheck the checkbox of the corresponding CPU number if any of the following CPU modules is used. • High Performance model QCPU • Process CPU • C Controller module (Q06CCPU-V or Q06CCPU-V-B) • PC CPU module	All items selected

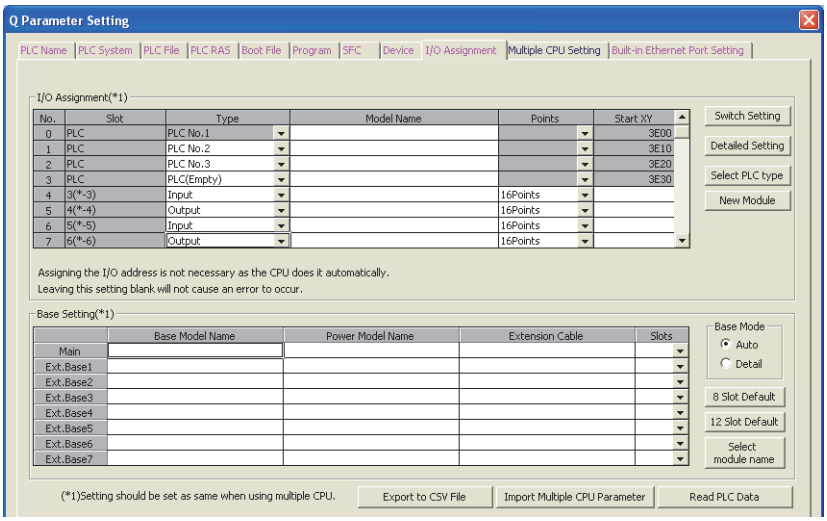
Item	Description	Default
Online Module Change	(1) Basic model QCPU This parameter is not supported. (2) Process CPU Check the checkbox to enable online module change. (3) High Performance model QCPU and Universal model QCPU Check the checkbox if online module change is enabled with a Process CPU. Modules controlled by a High Performance model QCPU or Universal model QCPU cannot be replaced online.	Not selected
I/O Sharing When Using Multiple CPUs	Set this parameter to read the input (X) and output (Y) data from the I/O modules and intelligent function modules controlled by other CPU modules. • Loading input (X) data: Page 108, Section 5.2.1 • Loading output (Y) data: Page 110, Section 5.2.2	Not selected
Multiple CPU High Speed Transmission Area Setting	Set this parameter to enable automatic data communications between the CPU modules in the system using the multiple CPU high speed transmission area of the CPU shared memory. Only Universal model QCPUs support this parameter. Note that some conditions must be met on the main base units and CPU modules to be used. (Page 138, Section 6.1.2) If the conditions cannot be satisfied, use "Communication Area Setting (Refresh Setting)".	"Use Multiple CPU High Speed Transmission" checkbox: Selected
Communication Area Setting (Refresh Setting)	Set this parameter to enable automatic data communications between the CPU modules in the system using the automatic refresh area of the CPU shared memory. (Page 125, Section 6.1.1)	-

Point

Match "No. of PLC" with the number of CPU modules actually mounted. If the numbers do not match, an error will occur.

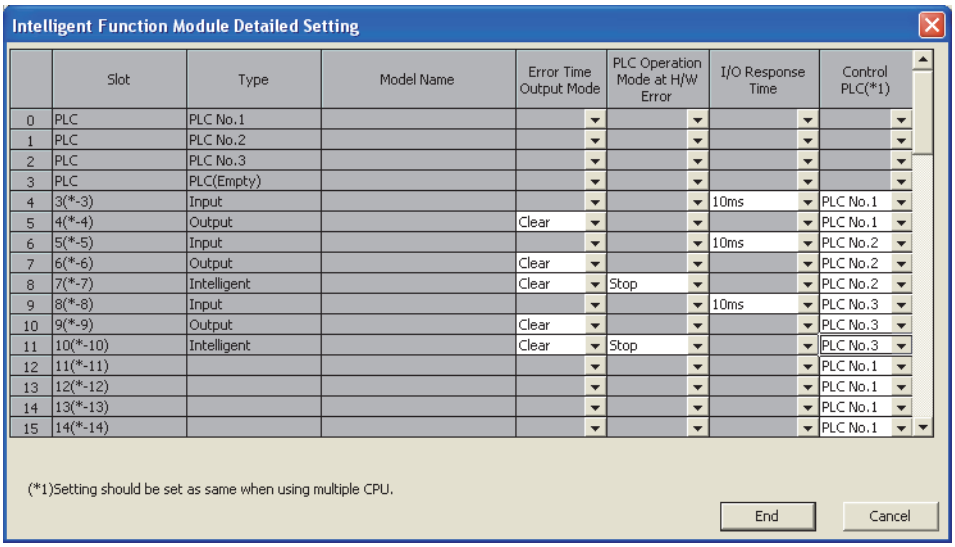
3. Set the types and points for the mounted modules in the "I/O Assignment" window of PLC parameter.

Project window ⇨ [Parameter] ⇨ [PLC Parameter] ⇨ [I/O Assignment]



Item	Description	Default
Type	Select the type of a mounted module. To reserve an empty slot for the future addition of a CPU module, select "PLC (Empty)". The slots where "PLC (Empty)" can be set differ depending on the CPU module used as CPU No.1. • When a Basic model QCPU is used as CPU No.1 ☞ Page 40, Section 3.1.2 (2) (d) • When a High Performance model QCPU or Process CPU is used as CPU No.1 ☞ Page 52, Section 3.2.2 (2) (f) • When a Universal model QCPU is used as CPU No.1 ☞ Page 67, Section 3.3.2 (2) (f)	-
Model Name	Enter the model name of a mounted module. This is a memo in the programming tool and does not affect the operation of CPU modules.	Blank
Points	Set the number of I/O points for each module.	Blank

4. **Click the Detailed Setting button in the "I/O Assignment" window, and set a control CPU for each I/O module and intelligent function module.**



Item	Description	Default
Control PLC	Set the CPU module that controls each I/O module and intelligent function module mounted.	PLC No.1

5. **Set other parameters required.**

6. **Save the project using the programming tool so that the multiple CPU system parameter settings can be used in other CPU modules.**

[Project] ⇨ [Save As]

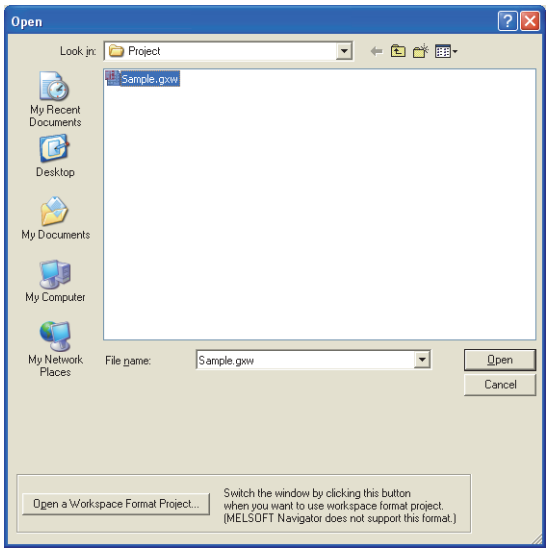
(2) Using the multiple CPU system parameters set to another CPU module

1. Click the [Import Multiple CPU Parameter] button in the "Multiple CPU Setting" window of PLC parameter.

Select and open the project file from which the settings will be imported.

Project window ⇨ [Parameter] ⇨ [PLC Parameter] ⇨ [Multiple CPU Setting]

⇨ [Import Multiple CPU Parameter]



Point

The settings of a project file created with a different programming tool cannot be used. Reuse such settings as follows.

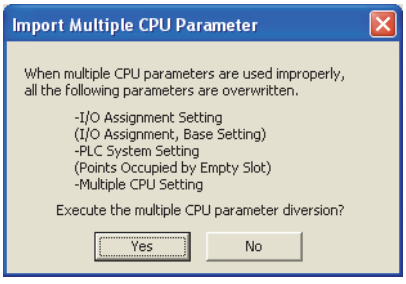
- To import the settings of a project file created with GX Developer to GX Works2, open the GX Developer project in GX Works2 by using the [Open Other Project] function.

[Project]⇨[Open Other Data]⇨[Open Other Project]

- To import the settings of a project file created with GX Works2 to GX Developer, save the GX Works2 project in the GX Developer format by using [Export to GX Developer Format File] function.

[Project] ⇨ [Export to GX Developer Format File]

2. The following window appears. Click the [Yes] button.



3. Check the settings in the "Multiple CPU Setting" window of PLC parameter.

To change the auto refresh setting devices, click the [Refresh] button and set new device ranges. (Settings of parameters with "(*1)" must be the same in all the CPU modules in the system.)

4. **Check the "Points Occupied by Empty Slot" setting in the "PLC System" window of PLC parameter.**

Project window ⇨ [Parameter] ⇨ [PLC parameter] ⇨ [PLC System] ⇨ "Points Occupied by Empty slots"

5. **Check the settings in the "I/O Assignment" window of PLC parameter.**

Project window ⇨ [Parameter] ⇨ [PLC parameter] ⇨ [I/O Assignment]

6. **Click the** Detailed Setting **button in the "I/O Assignment" window and check the "Control PLC" setting.**

7. **Set other parameters required.**

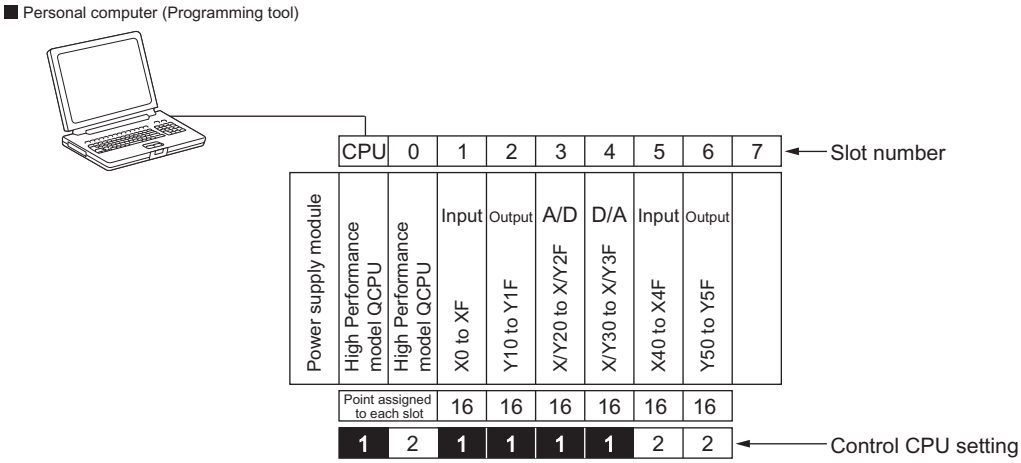
8. **Save the project using the programming tool.**

[Project] ⇨ [Save As]

4.3 Program Examples for Communications by Auto Refresh

4.3.1 Program examples for Basic model QCPU, Qn(H)CPU, and QnPHCPU

This section provides program examples for communicating data by auto refresh between the CPU modules in the following system.

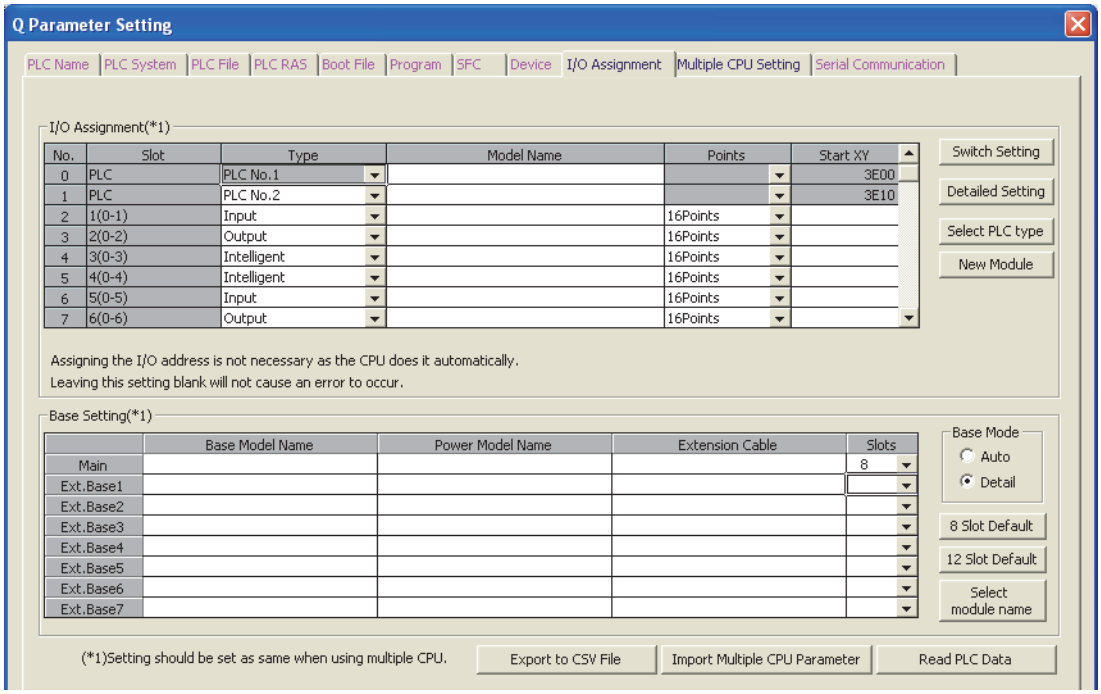


(1) Parameter settings

(a) I/O assignment

Assign I/O points to the mounted modules. (Page 29, Section 2.2)

Project window ⇨ [Parameter] ⇨ [PLC Parameter] ⇨ [I/O Assignment]



(b) Auto refresh setting

Set auto refresh parameters. (☞Page 126, Section 6.1.1 (2))

Project window ⇨ [Parameter] ⇨ [PLC Parameter] ⇨ [Multiple CPU Setting] ⇨ "Communication Area Setting (Refresh Setting)"

Change Screens: Setting 1

PLC	CPU Specific Send Range			PLC Side Device	
	Auto Refresh Area Caution)			Start Device	D0
	Points(*1)	Start	End	Start	End
PLC No.1	32	0000	001F	D0	D31
PLC No.2	32	0000	001F	D32	D63
PLC No.3					
PLC No.4					

Change Screens: Setting 2

PLC	CPU Specific Send Range			PLC Side Device	
	Auto Refresh Area Caution)			Start Device	M0
	Points(*1)	Start	End	Start	End
PLC No.1	2	0020	0021	M0	M31
PLC No.2	2	0020	0021	M32	M63
PLC No.3					
PLC No.4					

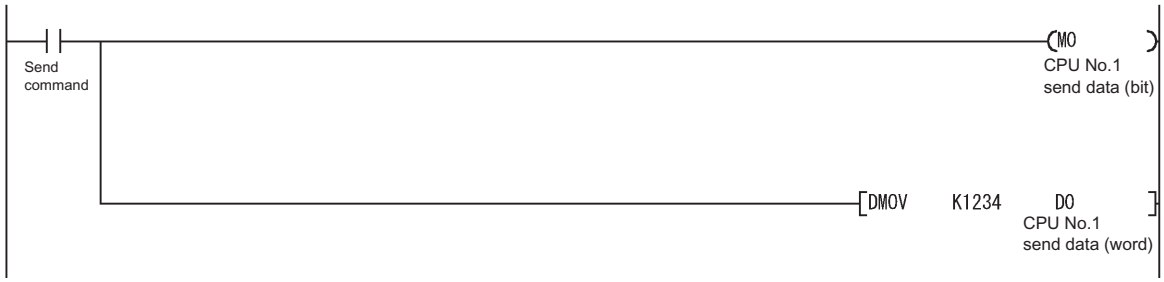
(2) Program examples

(a) Sending bit data and word data from CPU No.1 to CPU No.2

• Devices used in CPU modules

Device used in CPU No.1		Device used in CPU No.2	
M0	Send data from CPU No.1 to CPU No.2	M0	Send data from CPU No.1 to CPU No.2
D0 and D1		D0 and D1	
-		D100	Storage device for data received from CPU No.1
		YE0	Data reception flag (for data from CPU No.1)
		SM400	Always ON

• Program example of CPU No.1



• Program example of CPU No.2

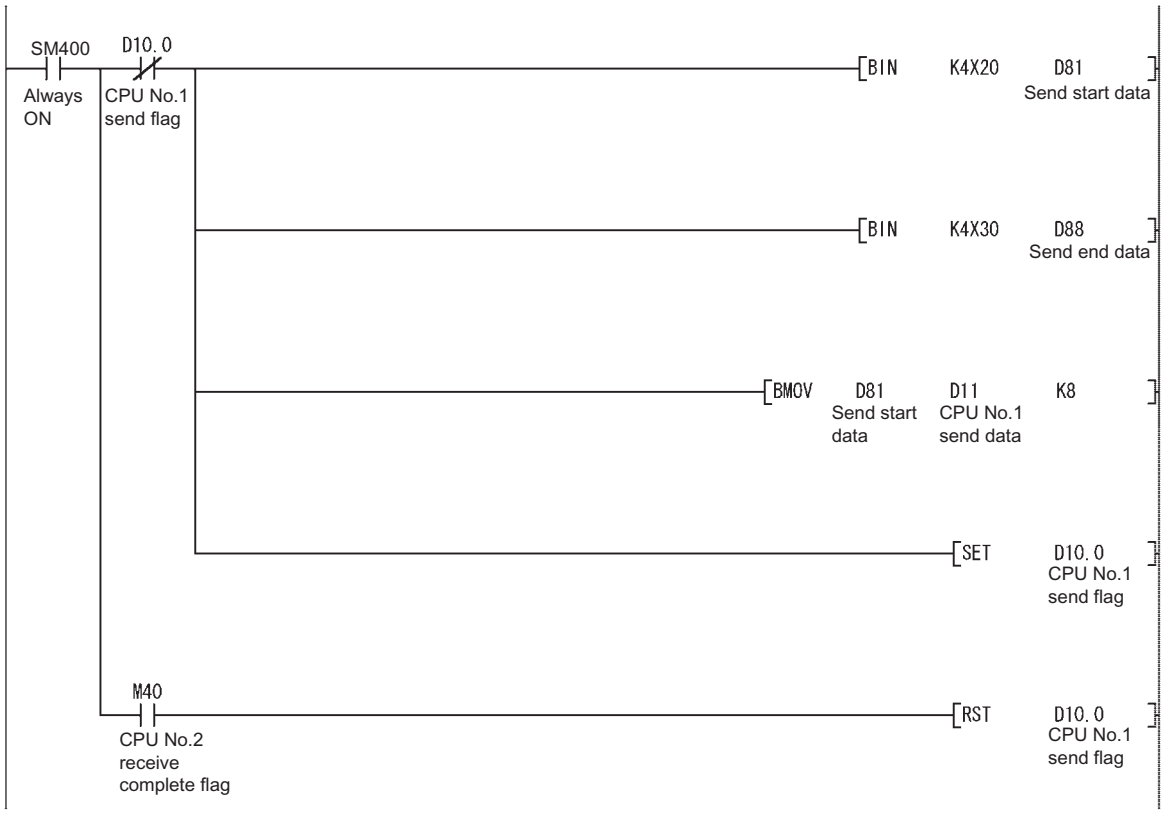
(b) Continuously sending data from CPU No.1 to CPU No.2

• Devices used in CPU modules

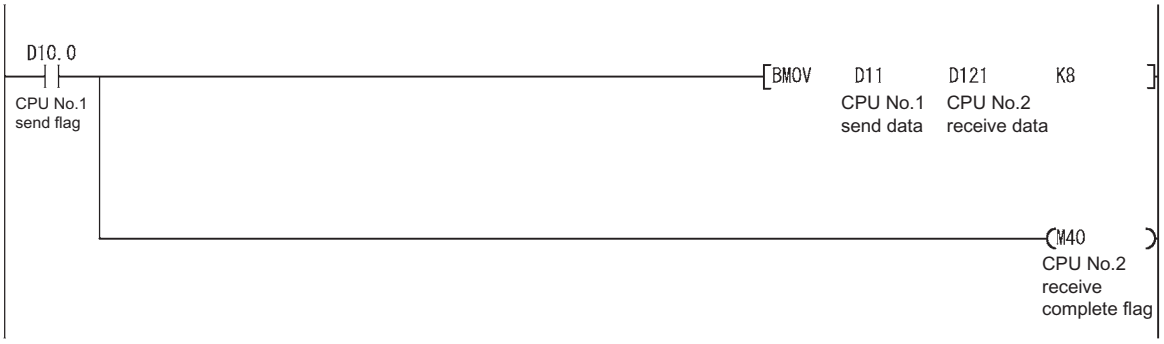
Device used in CPU No.1		Device used in CPU No.2	
M40	Send data from CPU No.2 to CPU No.1	M40	Send data from CPU No.2 to CPU No.1
D10 to D18	Send data from CPU No.1 to CPU No.2	D10 to D18	Send data from CPU No.1 to CPU No.2
D81 to D88	Storage device of send data to CPU No.2	D121 to D128	Storage device for data received from CPU No.1
SM400	Always ON	-	

For handshake between CPU No.1 and No.2, refer to Page 135, Section 6.1.1 (3).

• Program example of CPU No.1



• Program example of CPU No.2



(c) Continuously reading/writing data between CPU No.1 and No.2 using the user setting area

Data can be read/write between CPU modules by programs using the user setting area in the CPU shared memory.

Point

The same number of points must be set for CPU No.1 and CPU No.2 in the auto refresh setting.

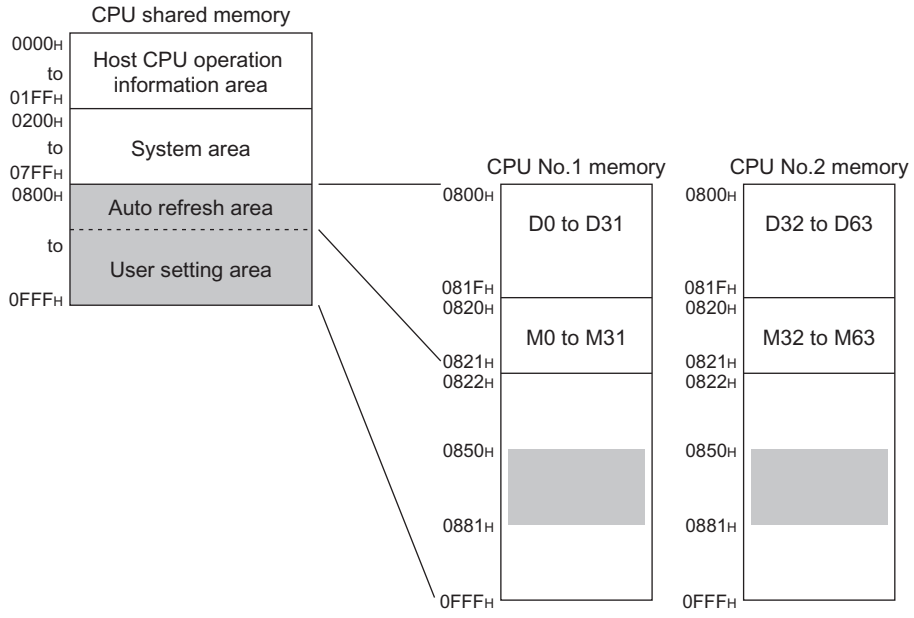
Change Screens: Setting 1

PLC	CPU Specific Send Range			PLC Side Device	
	Auto Refresh Area Caution)			Start Device	D0
	Points(*1)	Start	End	Start	End
PLC No.1	32	0000	001F	D0	D31
PLC No.2	32	0000	001F	D32	D63
PLC No.3					
PLC No.4					

Change Screens: Setting 2

PLC	CPU Specific Send Range			PLC Side Device	
	Auto Refresh Area Caution)			Start Device	M0
	Points(*1)	Start	End	Start	End
PLC No.1	2	0020	0021	M0	M31
PLC No.2	2	0020	0021	M32	M63
PLC No.3					
PLC No.4					

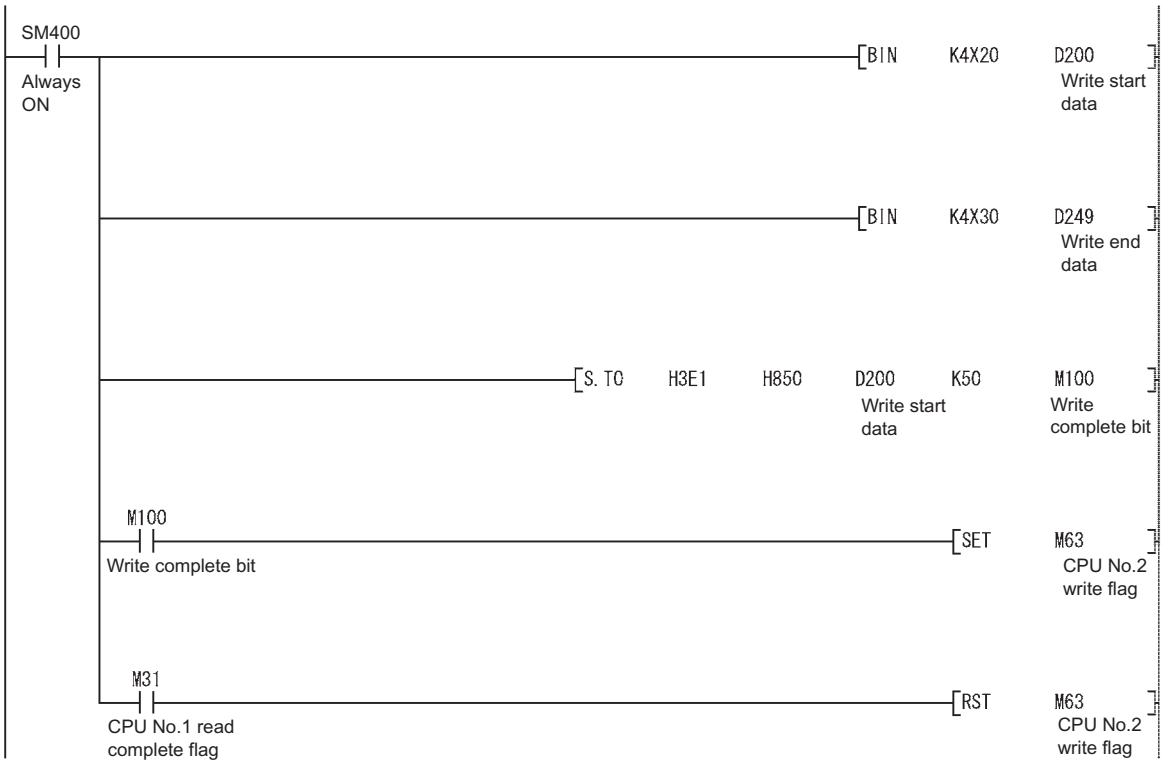
The auto refresh area occupies the memory addresses 0800_H to 0821_H, the area set by setting 1 and setting 2. Consequently, the user setting area will be a range from 0822_H to $0FFF_H$. (☞ Page 121, Section 6.1)



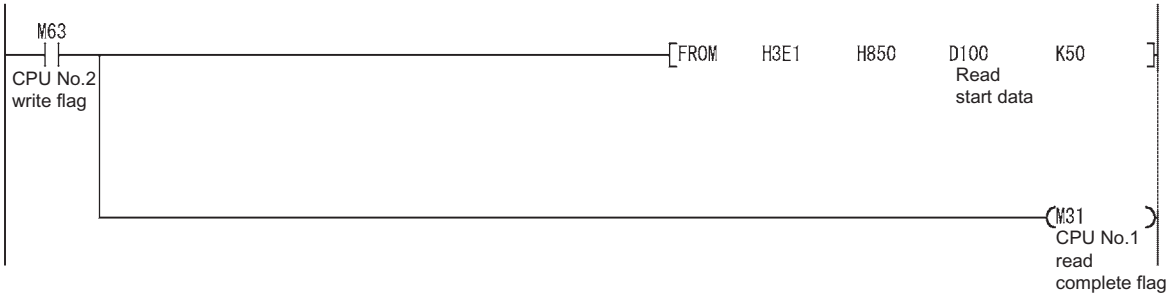
• Devices used in CPU modules

Device used in CPU No.1		Device used in CPU No.2	
M31	Send data from CPU No.1 to CPU No.2	M31	Send data from CPU No.1 to CPU No.2
M63	Send data from CPU No.2 to CPU No.1	M63	Send data from CPU No.2 to CPU No.1
D100 to D149	Storage device for data received from CPU No.2	D200 to D249	Storage device of send data to CPU No.1
-		M100	Write completion bit of the S.TO instruction
		SM400	Always ON

• Program example of CPU No.2

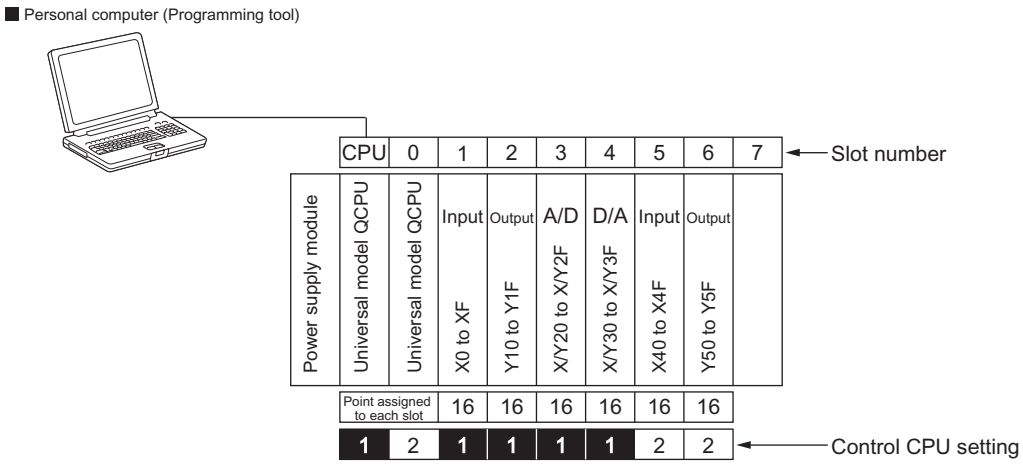


• Program example of CPU No.1



4.3.2 Program examples for Universal model QCPU

This section provides program examples for communicating data by auto refresh (using the multiple CPU high speed transmission area) between the CPU modules in the following system.

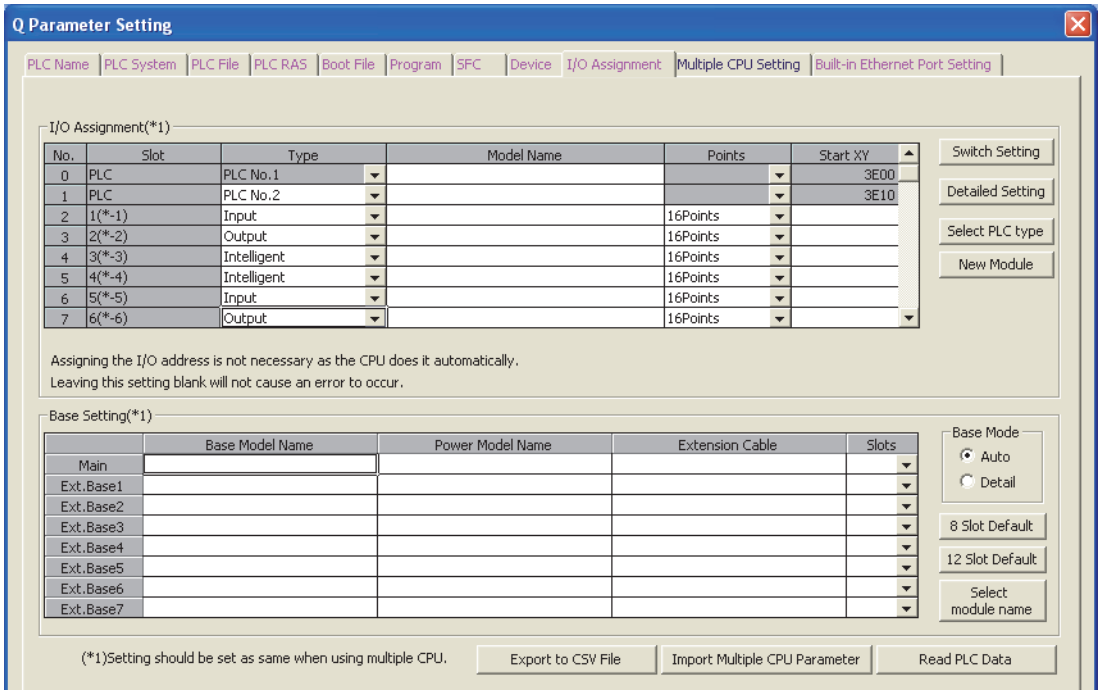


(1) Parameter settings

(a) I/O assignment

Assign I/O points to the mounted modules. (Page 29, Section 2.2)

Project window ⇨ [Parameter] ⇨ [PLC Parameter] ⇨ [I/O Assignment]

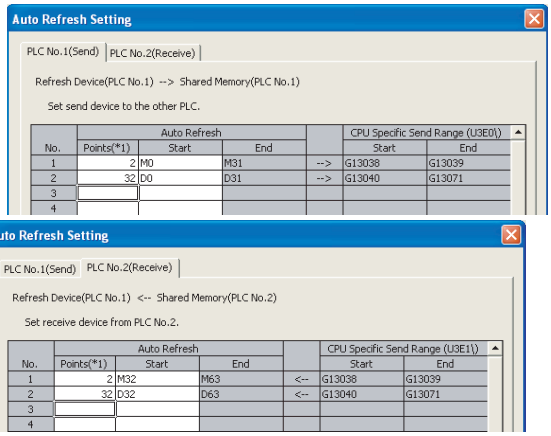


(b) Auto refresh setting

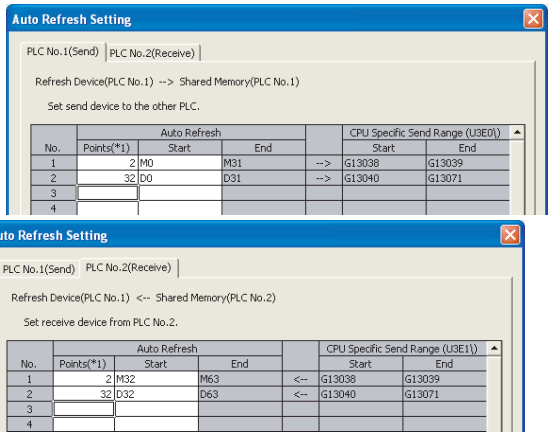
Set auto refresh parameters. (Page 141, Section 6.1.2 (3))

Project window ⇨ [Parameter] ⇨ [PLC Parameter] ⇨ [Multiple CPU Setting] ⇨ "Multiple CPU High Speed Transmission Area Setting"

Setting of CPU No.1



Setting of CPU No.2



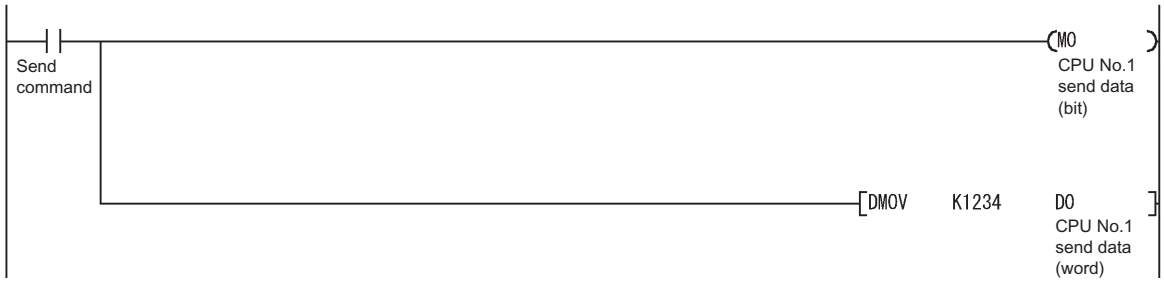
(2) Program examples

(a) Sending bit data and word data from CPU No.1 to CPU No.2

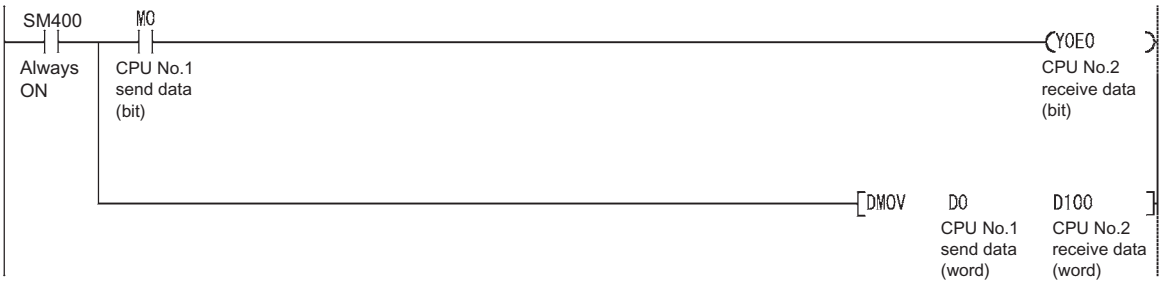
• Devices used in CPU modules

Device used in CPU No.1		Device used in CPU No.2	
M0	Send data from CPU No.1 to CPU No.2	M0	Send data from CPU No.1 to CPU No.2
D0 and D1		D0 and D1	
-		D100	Storage device for data received from CPU No.1
		YE0	Data reception flag (for data from CPU No.1)
		SM400	Always ON

• Program example of CPU No.1



• Program example of CPU No.2



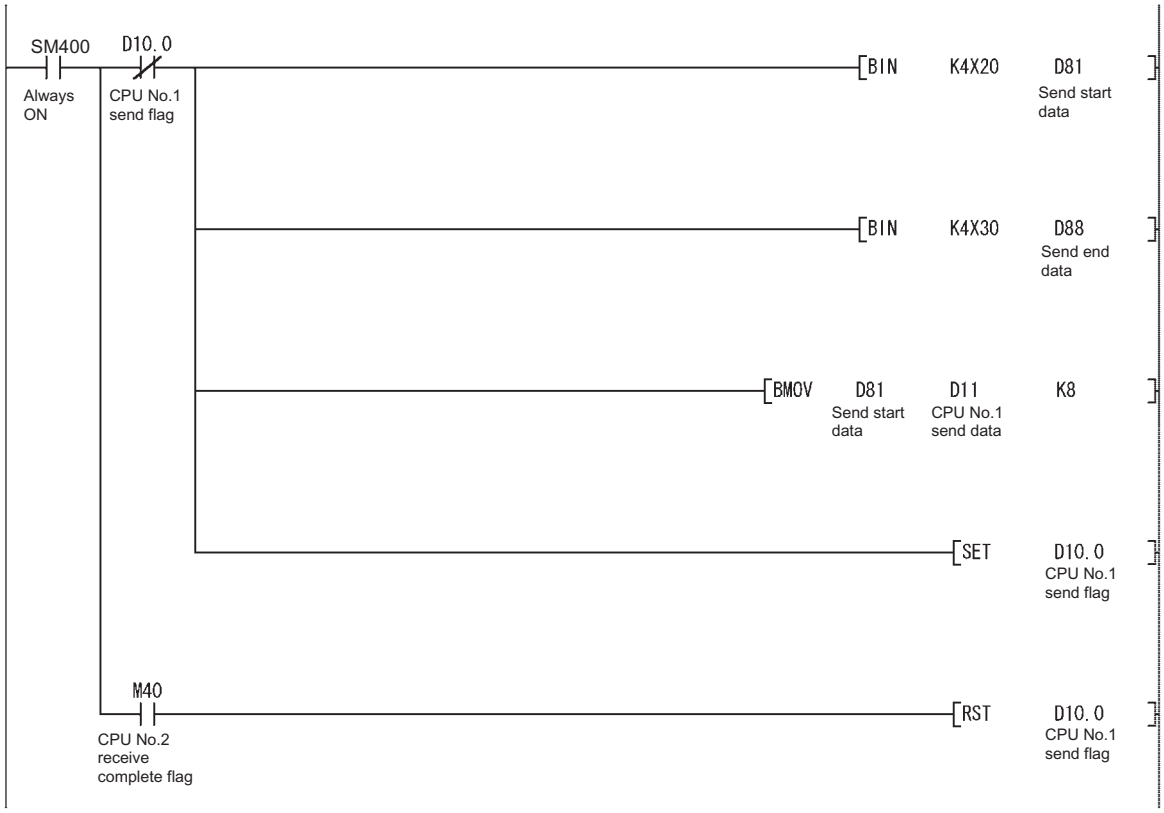
(b) Continuously sending data from CPU No.1 to CPU No.2

• Devices used in CPU modules

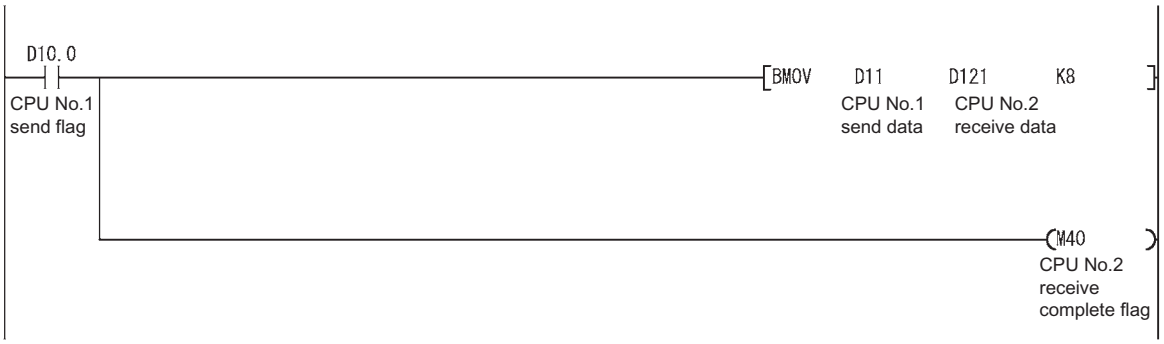
Device used in CPU No.1		Device used in CPU No.2	
M40	Send data from CPU No.2 to CPU No.1	M40	Send data from CPU No.2 to CPU No.1
D10 to D18	Send data from CPU No.1 to CPU No.2	D10 to D18	Send data from CPU No.1 to CPU No.2
D81 to D88	Storage device of send data to CPU No.2	D121 to D128	Storage device for data received from CPU No.1
SM400	Always ON	-	

For handshake between CPU No.1 and No.2, refer to Page 151, Section 6.1.2 (5).

• Program example of CPU No.1



• Program example of CPU No.2



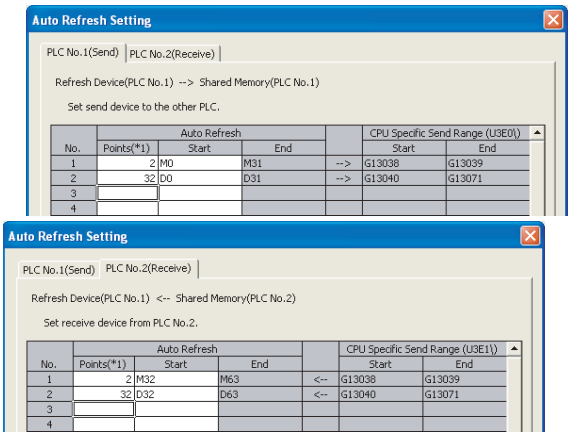
(c) Continuously reading/writing data between CPU No.1 and CPU No.2 using the user setting area in the multiple CPU high speed transmission area

Data can be read/write between CPU modules using the user setting area in the CPU shared memory.

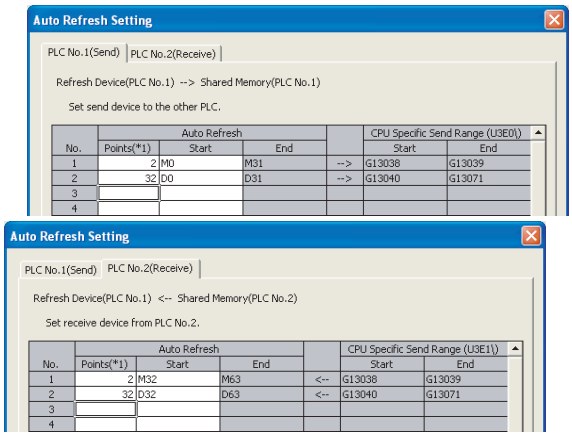
Point

The same number of points must be set for CPU No.1 and CPU No.2 in the auto refresh setting.

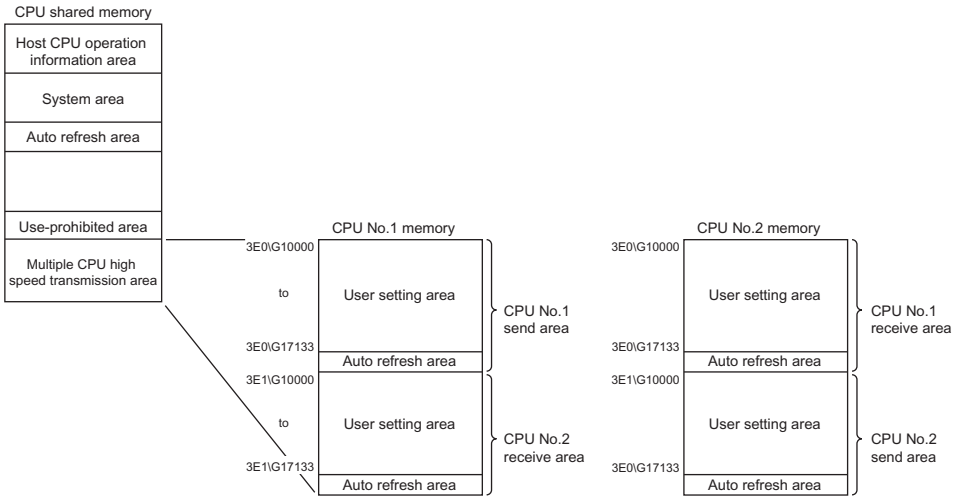
Setting of CPU No.1



Setting of CPU No.2



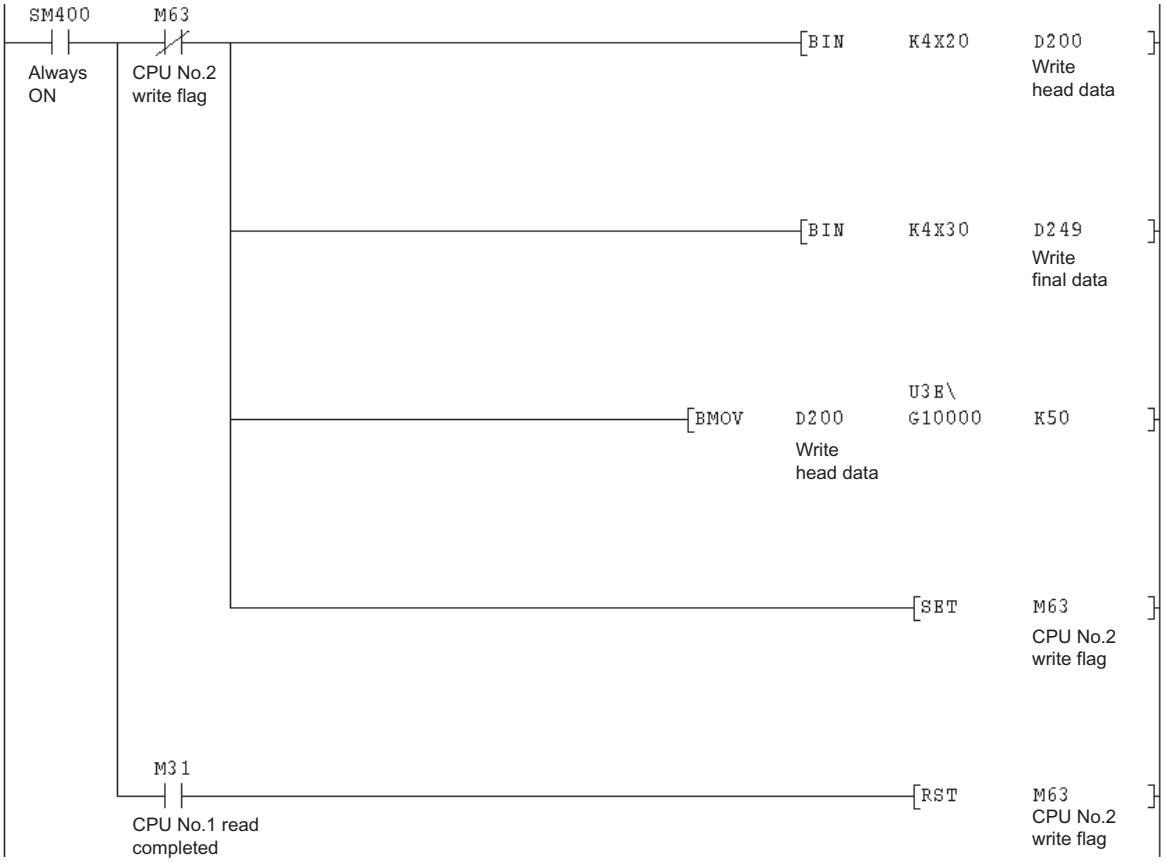
The user setting area will be 3E0\G10000 and later for CPU No.1 and 3E1\G10000 and later for CPU No.2.



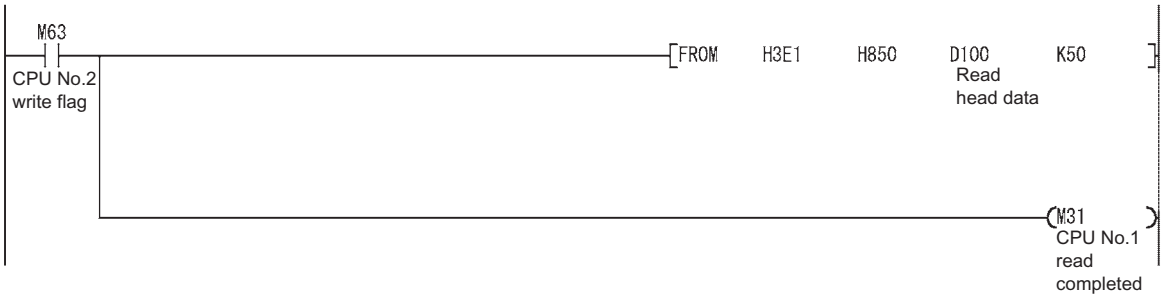
• Devices used in CPU modules

Device used in CPU No.1		Device used in CPU No.2	
M31	Send data from CPU No.1 to CPU No.2	M31	Send data from CPU No.1 to CPU No.2
M63	Send data from CPU No.2 to CPU No.1	M63	Send data from CPU No.2 to CPU No.1
D100 to D149	Storage device for data received from CPU No.2	D200 to D249	Storage device of send data to CPU No.1
-		SM400	Always ON

• Program example of CPU No.2



• Program example of CPU No.1



4.4 Clock Data

This section describes clock data of CPU modules and intelligent function modules.

4.4.1 Clock data of CPU modules

Set clock data to CPU No.1 in the multiple CPU system using the programming tool.

[Online] ⇨ [Set Clock]

The clock data settings for CPU No.2 to No.4 differ depending on the CPU module used.

CPU module	Setting of CPU No.2 to No.4
• Universal model QCPU • Motion CPU (Q172DCPU(-S1), Q173DCPU(-S1), Q172DSCPU, or Q173DSCPU) • C Controller module (Q12DCCPU-V, Q24DHCCPU-V, Q24DHCCPU-VG, Q24DHCCPU-LS, or Q26DHCCPU-LS)	Clock data do not need to be set. The clock data of CPU No.1 is automatically set to CPU No.2 to No.4. Even if clock data is set individually to CPU No.2 to No.4, the setting is ignored and the clock data of CPU No.1 is automatically set.
Other than above	Set clock data individually to CPU No.2 to No.4. The clock data of CPU No.1 is not automatically set to CPU No.2 to No.4.

Point

- Clock data can also be set by the following methods.
  - By a program
  - By executing the time setting function (SNTP client) (Only Built-in Ethernet port QCPUs support this function.)
- To automatically set the clock data of CPU No.1 to a C Controller module, perform the following operation.
  - When the Q12DCCPU-V is used
    Enable the clock synchronization function using C Controller setting utility. (The function is disabled by default.)

    C Controller setting utility [Online Operation] ⇨ "C Controller Module Detail Setting" ⇨ "Clock" ⇨ "Clock Synchronization Function"
  - When the Q24DHCCPU-V, Q24DHCCPU-VG, Q24DHCCPU-LS, or Q26DHCCPU-LS is used
    Clock data do not need to be set. The clock data of CPU No.1 is automatically set.
- If there is an error of three seconds or more between the clock data of the C Controller module (Q12DCCPU-V, Q24DHCCPU-V, Q24DHCCPU-VG, Q24DHCCPU-LS, or Q26DHCCPU-LS) and the clock data received from CPU No.1, the C Controller module synchronizes the clock data.

Remark

CPU No.1 sends clock data to other CPU modules at the following timing.
- When the multiple CPU system is powered on
- When the RUN/STOP switch of CPU No.1 is switched from STOP to RUN
- At intervals of one second after the multiple CPU system starts up

The clock data includes year, month, day, day of the week, hour, minute, and second information.
Since CPU No.1 sets the clock data at intervals of one second, an error of one second (maximum) may occur in clock data of CPU modules other than CPU No.1.

4.4.2 Clock data of intelligent function modules

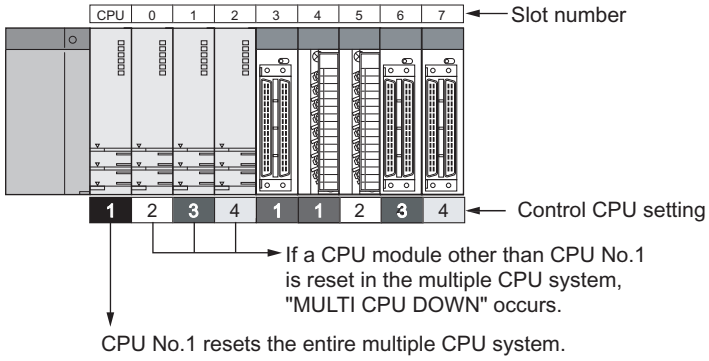
When an error has occurred, some intelligent function modules store the code and time (clock data read from the QCPU) corresponding to the error into the buffer memory. Those modules store the clock data of CPU No.1 as the error time regardless of whether the modules are controlled by CPU No.1 or not.

4.5 Resetting a Multiple CPU System

In a multiple CPU system, resetting the QCPU used as CPU No.1 resets all the modules (CPU modules, I/O modules, and intelligent function modules) in the system.

(1) If a stop error exists any of the CPU modules in the multiple CPU system

Reset CPU No.1 or power off and on the multiple CPU system. The system cannot be restored by resetting any CPU module other than CPU No.1.



Point

- Do not individually reset the CPU modules other than CPU No.1 in the multiple CPU system.
  If reset, "MULTI CPU DOWN" (error code: 7000) will occur and the entire multiple CPU system stops.
  - Depending on the timing in which any of CPU modules other than CPU No.1 is reset, an error other than "MULTI CPU DOWN" (error code: 7000) may occur, causing the other CPU modules to stop.
  - If any of CPU modules other than CPU No.1 is reset, "MULTI CPU DOWN" (error code: 7000) will occur regardless of the "Operation Mode" setting in PLC parameter ("Multiple CPU Setting").

4.6 System Operation When a Stop Error Occurs

The multiple CPU system operation differs depending on the CPU module where a stop error has occurred.

(1) When a stop error has occurred in CPU No.1

"MULTI CPU DOWN" (error code: 7000) occurs in all the other CPU modules and the operation of the multiple CPU system stops.

(2) When a stop error has occurred in a CPU module other than CPU No.1

The operating status of the system (whether to stop the entire system or not) depends on the "Operation Mode" setting in PLC parameter ("Multiple CPU Setting").

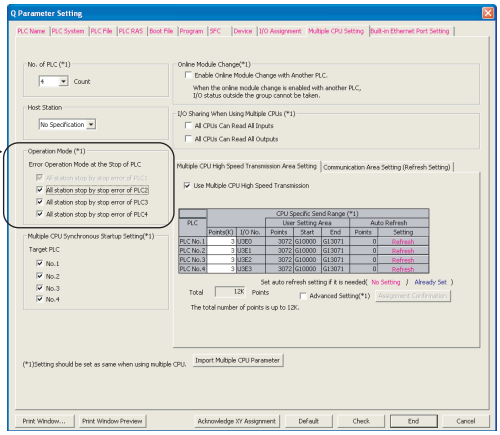
Parameters are set by default so that the operations of all the CPU modules stop.

To continue operations, uncheck the "All station stop by stop error of PLC 'n'" checkbox of the corresponding CPU module.

Operation Mode

☑ All Station stop by stop error of PLC 'n': Operations of all the other CPU modules stop when an error occurs in CPU No. n.

☐ All Station stop by stop error of PLC 'n': Operations of all the other CPU modules continue even if an error occurs in CPU No. n.



(a) When the "All station stop by stop error of CPU 'n'" checkbox is checked

If a stop error occurs in the CPU module for which "All station stop by stop error of PLC 'n'" has been set, "MULTI CPU DOWN" (error code: 7000) occurs in all the other CPU modules and the operation of the multiple CPU system stops.

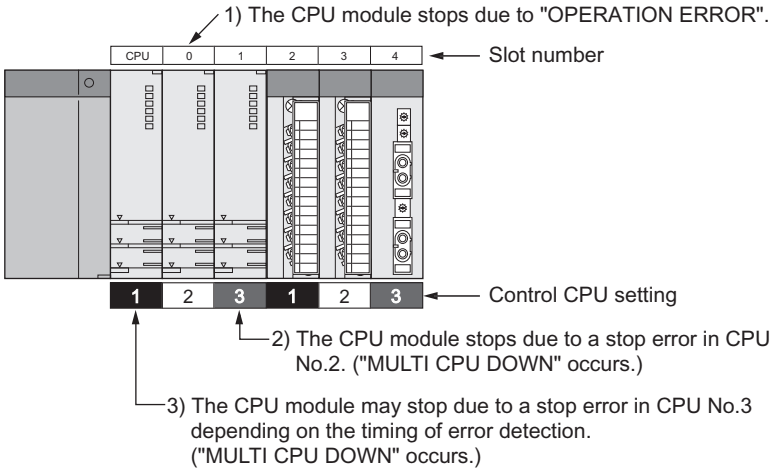
(b) When the "All station stop by stop error of CPU 'n'" checkbox is not checked

If a stop error occurs in the CPU module for which "All station stop by stop error of PLC 'n'" has not been set, "MULTI EXE. ERROR" (error code: 7020) occurs in all the other CPU modules, but the operation of the multiple CPU system continues.

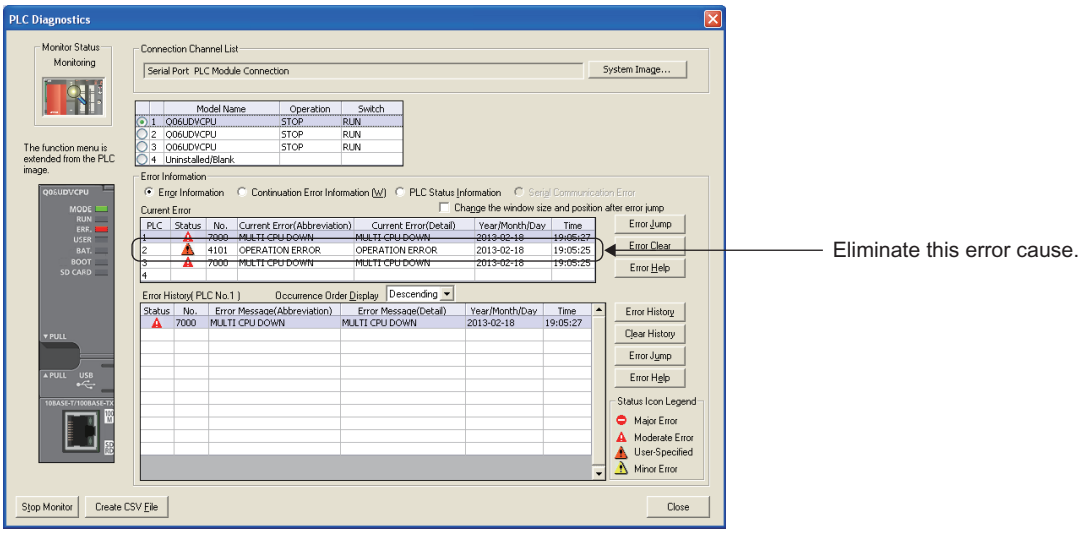
However, if a major error occurs in the CPU module 'n', "MULTI CPU DOWN" (error code: 7000) occurs in all the other CPU modules and the operation of the multiple CPU system stops regardless of the PLC parameter setting.

Point

If a stop error occurs, "MULTI CPU DOWN" (error code: 7000) will occur in the CPU module where the stop error has been detected. Depending on the timing of error detection, "MULTI CPU DOWN" may be detected in another CPU module due to secondary-occurred "MULTI CPU DOWN".
For example, if a stop error occurs in CPU No.2, the operation of CPU No.3 stops. Depending on the timing of error detection, the operation of CPU No.1 may stop due to the stop error of CPU No.3, not the error of CPU No.2.



Because of this, CPU No. different from the one of the first error CPU module may be stored in the common error information field. To restore the system, eliminate the error cause of the CPU module that has been stopped by an error other than "MULTI CPU DOWN".
In the following example, the error cause (other than "MULTI CPU DOWN") of CPU No.2 shall be eliminated.



(3) System restoration procedure

The following is the procedure for restoring the system.

1. **Check the error CPU No. and error cause in the "PLC diagnostics" window using the programming tool.**
2. **Eliminate the error cause.**
3. **Reset CPU No.1 or power off and on the system.**
   All the CPU modules in the multiple CPU system are reset and the system is restored.

CHAPTER 5 ACCESS BETWEEN CPU MODULES AND OTHER MODULES

This chapter describes the access between CPU modules and other modules (I/O modules and intelligent function modules).

5.1 Access to Controlled Modules

In a multiple CPU system, CPU modules access I/O modules and intelligent function modules in the same way as in a single CPU system. (CPU modules refresh input (X) and output (Y) data, and read/write data from/to the buffer memory of intelligent function modules.)

5.2 Access to Non-controlled Modules

Access to non-controlled modules is restricted as shown below.

○: Accessible ×: Inaccessible

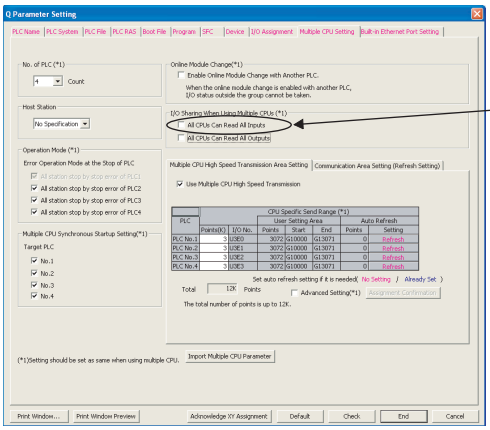
Access target		"I/O Sharing When Using Multiple CPUs" in PLC parameter	
		Disabled (not checked)	Enabled (checked)
Input (X)		×	○
Output (Y)	Read	×	○
	Write	×	×
Buffer memory of an intelligent function module	Read	○	○
	Write	×	×

Point

- The on/off data of the I/O modules, I/O combined modules, and intelligent function modules controlled by other CPU modules can be used as an interlock of the host CPU module or to check the status of output to external devices controlled by other CPU modules.
- The on/off status of input (X) and output (Y) can be read by setting "I/O Sharing When Using Multiple CPUs" in PLC parameter. (The on/off status cannot be written to the devices.)
- Data in the buffer memory of intelligent function modules can be read regardless of the "I/O Sharing When Using Multiple CPUs" setting. (The data cannot be written to the buffer memory.)

5.2.1 Loading input (X) data

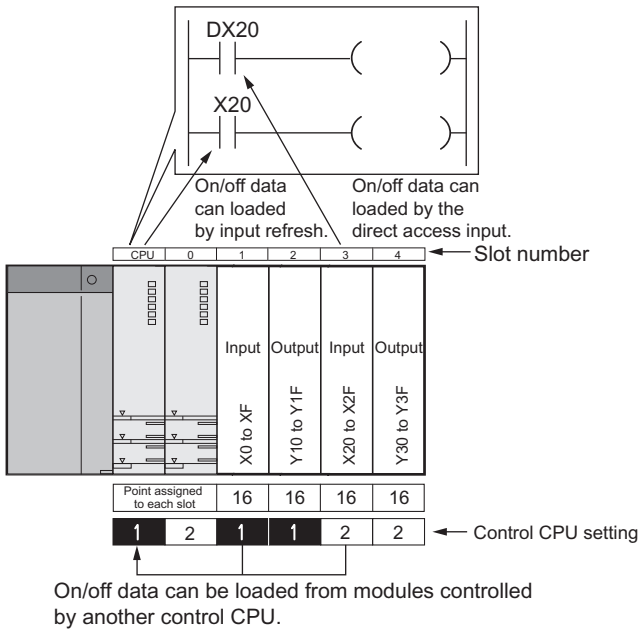
Data in the input (X) of input modules and intelligent function modules controlled by other CPU modules can be loaded in accordance with the "I/O Sharing When Using Multiple CPUs" setting in PLC parameter ("Multiple CPU Setting").



I/O Sharing When Using Multiple CPUs
☑ All CPUs Can Read All Inputs:
Input data can be loaded from the modules controlled by other CPU modules.
☐ All CPUs Can Read All Inputs:
Input data cannot be loaded from the modules controlled by other CPU modules.

(1) When the "All CPUs Can Read All Inputs" checkbox is checked

The on/off data of input modules and intelligent function modules controlled by other CPU modules can be loaded. The on/off data are loaded during input refresh processing before the program operation starts. The on/off data can also be loaded by using the direct access input (DX).

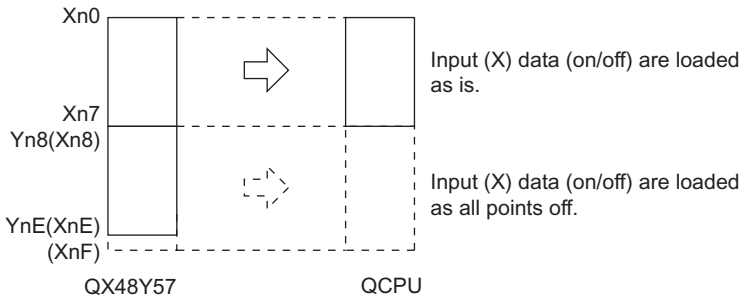


(a) Modules that can load input (X) data

Data in the input (X) can be loaded from the following modules mounted on the main base unit or extension base unit.

Module type set in PLC parameter ("I/O Assignment")	Mounted module
Blank	Input module
	High-speed input module
	I/O combined module*1
	Intelligent function module
Input Hi, Input I/O Mix	Input module
	High speed input module
	Output module*2
	I/O combined module*1
Intelligent	Intelligent function module

*1 When input (X) of the QX48Y57 (I/O combined module) is targeted, data in Xn8 to XnF (output part) are loaded as all points off.



*2 When input (X) of an output module is targeted, data are loaded as all points off.

(b) Modules that cannot load input (X) data

Input data of empty slots and MELSECNET/H or CC-Link network remote stations controlled by other CPU modules cannot be loaded. To use the input data (on/off data) in a CPU module other than the control CPU, perform auto refresh using the CPU shared memory. (Page 121, Section 6.1)

Point

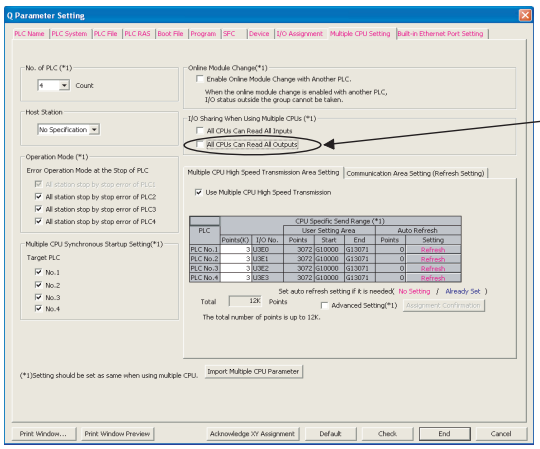
If the input data loaded from other CPU modules are forcibly turned on/off in the host CPU module, the data will be set into the specified forced on/off status. (User's Manual (Function Explanation, Program Fundamentals) for the CPU module used)

(2) When the "All CPUs Can Read All Inputs" checkbox is not checked

The on/off data of input modules and intelligent function modules controlled by other CPU modules cannot be loaded. Data in the input (X) remain at off.

5.2.2 Loading output (Y) data

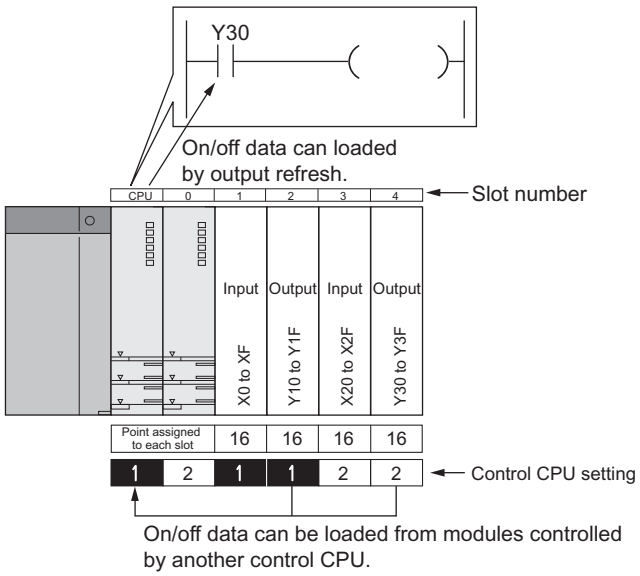
Data in the output (Y) of output modules and intelligent function modules controlled by other CPU modules can be loaded in accordance with the "I/O Sharing When Using Multiple CPUs" setting in PLC parameter ("Multiple CPU Setting").



I/O Sharing When Using Multiple CPUs
☑ All CPUs Can Read All Outputs:
Output data can be loaded from the modules controlled by other CPU modules.
☐ All CPUs Can Read All Outputs:
Output data cannot be loaded from the modules controlled by other CPU modules.

(1) When the "All CPUs Can Read All Outputs" checkbox is checked

The on/off data of output modules and intelligent function modules controlled by other CPU modules can be loaded to the output (Y) of the host CPU module.



(a) Modules that can load output (Y) data

Data in the output (Y) can be loaded from the following modules mounted on the main base unit or extension base unit.

Module type set in PLC parameter ("I/O Assignment")	Mounted module
Blank	Output module
	I/O combined module
	Intelligent function module
Output I/O Mix	Input module
	Output module
	I/O combined module
Intelligent	Intelligent function module

(b) Modules that cannot load output (Y) data

Output data of empty slots and MELSECNET/H or CC-Link network remote stations controlled by other CPU modules cannot be loaded. To use the output data in a CPU module other than the control CPU, perform auto refresh using the CPU shared memory and send the output data of remote stations from the control CPU to other CPU modules. (☞Page 121, Section 6.1)

Point

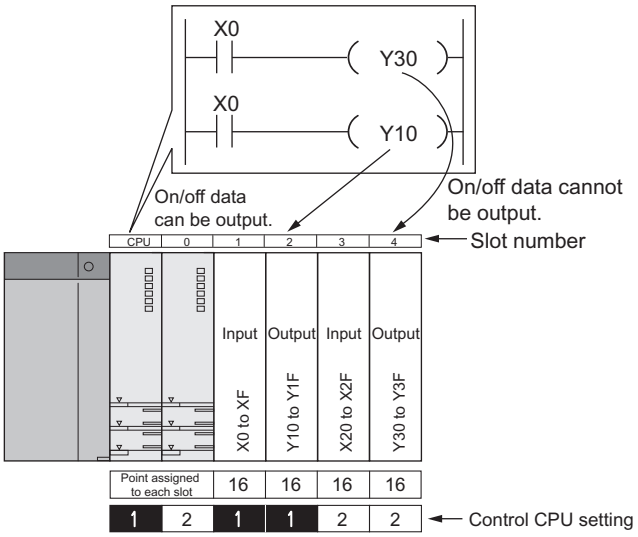
If the output loaded from other CPU modules is forcibly turned on/off in the host CPU module, the data will be set into the specified forced on/off status. (User's Manual (Function Explanation, Program Fundamentals) for the CPU module used)

(2) When the "All CPUs Can Read All Outputs" checkbox is not checked

The on/off data of output modules and intelligent function modules controlled by other CPU modules cannot be loaded. Data in the output (Y) remain at off.

5.2.3 Output to output modules and intelligent function modules

The on/off data cannot be output to non-controlled modules.
If the output status of the output module or intelligent function module controlled by other CPU modules is turned on/off by the program, the corresponding output status changes only within the CPU module. (The on/off data is not output to the corresponding output module or intelligent function module.)

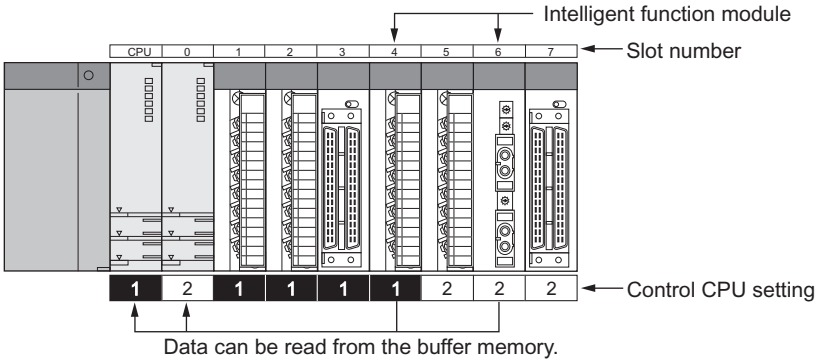


5.2.4 Access to the intelligent function module buffer memory

Data in the buffer memory of intelligent function modules controlled by other CPU modules can be read regardless of the "I/O Sharing When Using Multiple CPUs" setting in PLC parameter ("Multiple CPU Setting").

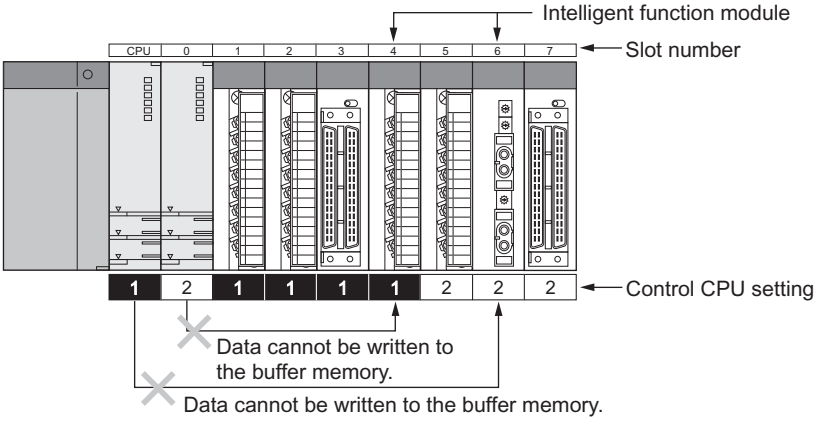
(1) Reading data from the buffer memory

Data can be read from the buffer memory of intelligent function modules controlled by other CPU modules in the same way as in a single CPU system.



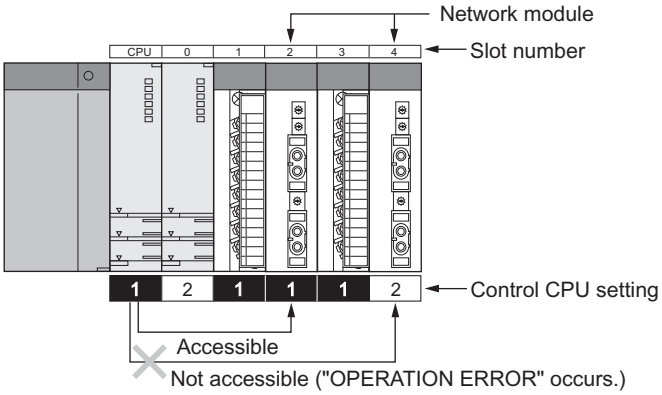
(2) Writing data to the buffer memory

Data cannot be written to the buffer memory of intelligent function modules.
If data is written to the buffer memory of an intelligent function module controlled by another CPU module, "SP.UNIT ERROR" (error code: 2116) occurs.



5.2.5 Access using the link direct device

Only the control CPU can execute instructions using the link direct device to access I/O modules and intelligent function modules.
The link direct device cannot be used to access modules controlled by other CPU modules. If an instruction using the link direct device is executed to access a module controlled by another CPU module , "OPERATION ERROR" (error code: 4102) occurs.



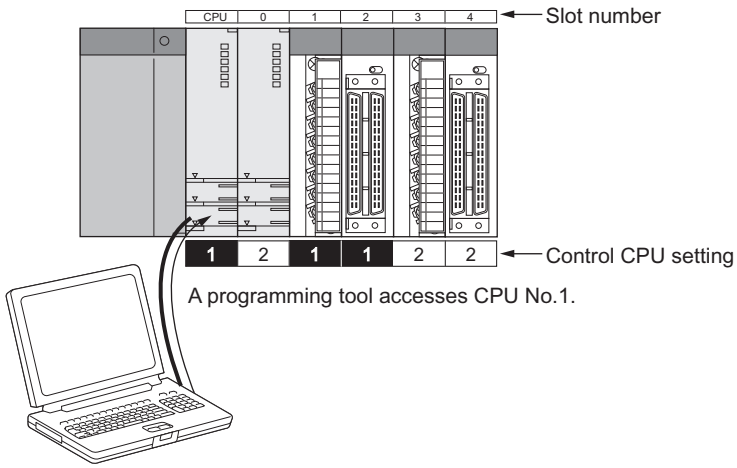
5.3 Access From a Programming Tool

This section describes access from a programming tool to modules in a multiple CPU system.

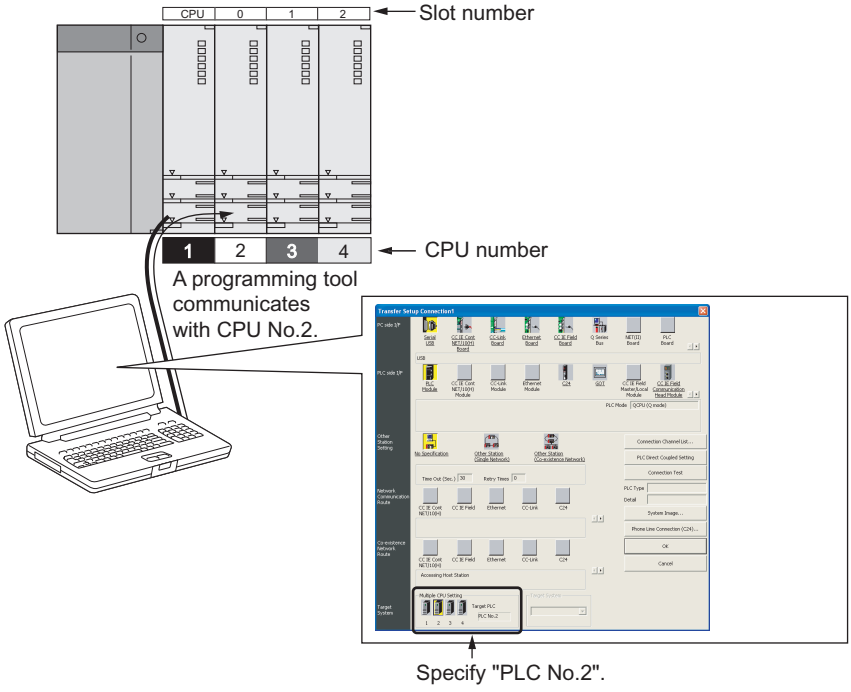
(1) Access to QCPUs

A programming tool can read/write parameters and programs from/to the QCPU connected as well as monitor and test the entire system. To access another QCPU via the QCPU connected, specify the target CPU No. in "Multiple CPU Setting" on the "Transfer Setup" window.

(a) When the target CPU module is not specified

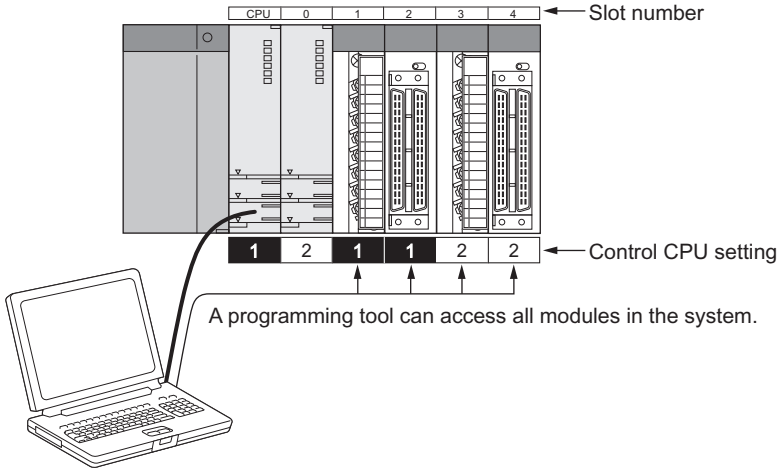


(b) When the target CPU module is specified



(2) Access to controlled and non-controlled modules

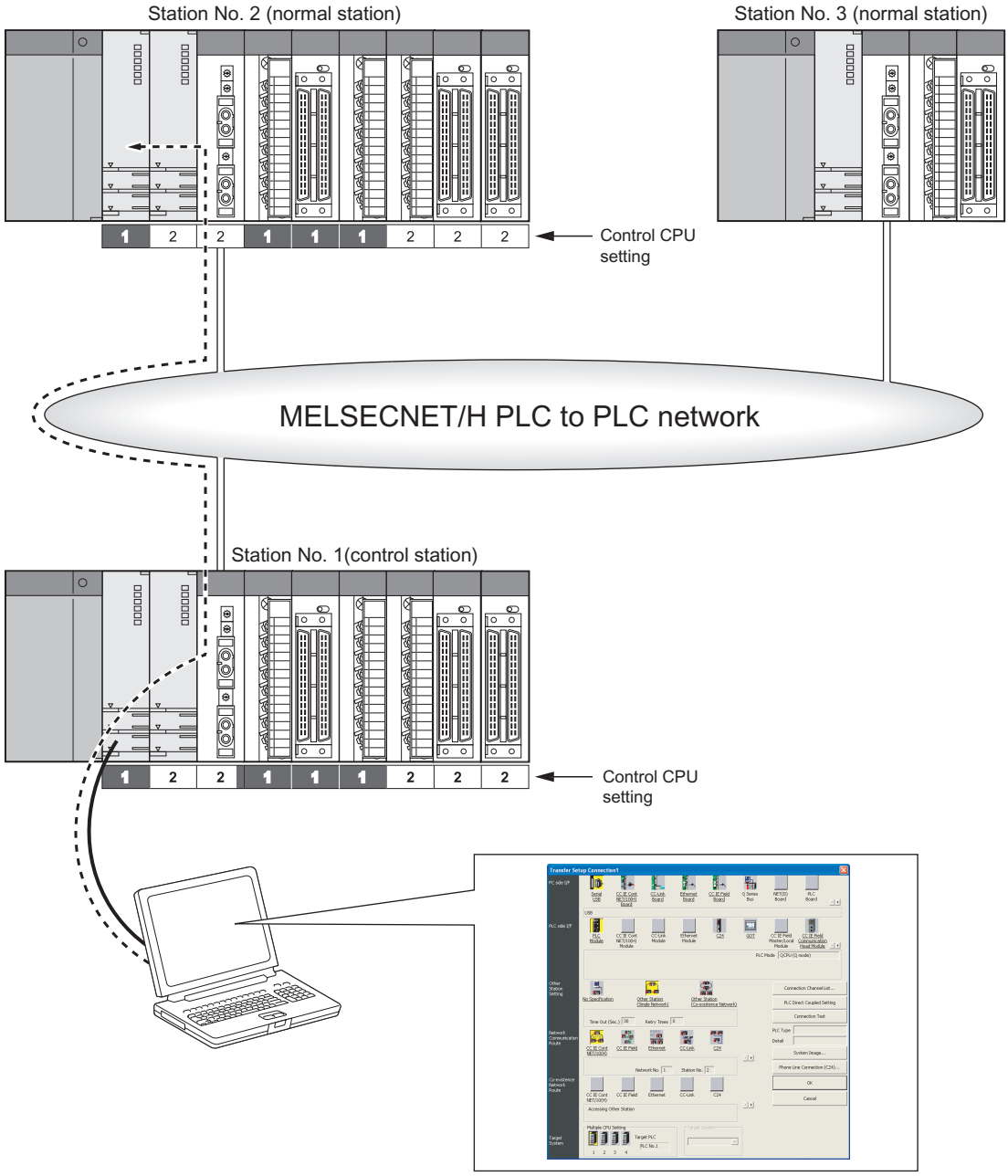
A programming tool can access modules both controlled and not controlled by the QCPU connected.
The programming tool connected to one QCPU can access all the modules controlled by any QCPU in the multiple CPU system.
The programming tool can also access QCPUs on other stations in the same network such as CC-Link IE, MELSECNET/H, or Ethernet.



(3) Access from the programming tool connected to another station

The programming tool connected to another station in the same network can access all the QCPUs in the multiple CPU system.

Ex. Over MELSECNET/H PLC to PLC network



5.4 Accessible QCPUs when GOT is connected

For the connected GOT, QCPUs that can be accessed differ depending on the connection method. (Manual for the GOT used)

CHAPTER 6 COMMUNICATIONS AMONG CPU MODULES

This chapter describes data communications among CPU modules in a multiple CPU system.

(1) Communication methods

The following table lists the communication methods available among CPU modules.

Item		Description	Reference
Communications using the CPU shared memory		Data communications is performed among CPU modules using the internal memory of each CPU module.	Page 121, Section 6.1
	Auto refresh (using the auto refresh area)	Data communications is automatically performed among CPU modules in accordance with the settings in the programming tool.	Page 125, Section 6.1.1
	Auto refresh (using the multiple CPU high-speed transmission area)		Page 138, Section 6.1.2
	By programs	Data communications is performed among CPU modules by executing programs.	Page 153, Section 6.1.3
Communications by motion dedicated instructions		Data communications is performed between a QCPU and a Motion CPU by executing motion dedicated instructions.	Page 163, Section 6.2
Communications among CPU modules by dedicated instructions		Data communications is performed among CPU modules by executing dedicated instructions.	–
	Reading/writing device data between QCPU and Motion CPU	Device data are read/written between a QCPU and a Motion CPU.	Page 165, Section 6.3.1
	Starting an interrupt program from QCPU to C Controller module/PC CPU module	An interrupt program is started from a QCPU to a C Controller module/PC CPU module.	Page 167, Section 6.3.2
	Reading/writing device data between QCPUs	Device data are read/written between Universal model QCPUs (except the Q00UCPU, Q01UCPU, and Q02UCPU).	Page 168, Section 6.3.3

(2) Communications among CPU modules

Communications availability differs depending on the CPU modules used as the communication source and target.

○: Communications available ×: Communications not available

Communication-source CPU module	Communication-target CPU module		Communications using the CPU shared memory		Communications by motion dedicated instructions*1	Communications among CPU modules by dedicated instructions
			Auto refresh	Program		
Basic model QCPU	Motion CPU	Q172CPUN(-T), Q173CPUN(-T), Q172HCPU(-T), Q173HCPU(-T)	○	○	○	○
	C Controller module		○	○	×	○
	PC CPU module		○	○	×	○
High Performance model QCPU, Process CPU	High Performance model QCPU, Process CPU, Universal model QCPU		○	○	×	×
	Motion CPU	Q172CPUN(-T), Q173CPUN(-T), Q172HCPU(-T), Q173HCPU(-T)	○	○	○	○
	C Controller module		○	○	×	○
	PC CPU module		○	○	×	○
Universal model QCPU (Q00UCPU, Q01UCPU, Q02UCPU)	Motion CPU	Q172CPUN(-T), Q173CPUN(-T), Q172HCPU(-T), Q173HCPU(-T)	○	○	○	○
	C Controller module	Q06CCPU-V, Q06CCPU-V-B, Q12DCCPU-V, Q24DHCCPU-V, Q24DHCCPU-VG, Q24DHCCPU-LS, Q26DHCCPU-LS	○	○	×	○
	PC CPU module		○	○	×	○
Universal model QCPU (Except the Q00UCPU, Q01UCPU, and Q02UCPU)	High Performance model QCPU, Process CPU		○	○	×	×
	Universal model QCPU		○	○	×	○
	Motion CPU	Q172DCPU(-S1), Q173DCPU(-S1), Q172DSCPU, Q173DSCPU	○	○	○	○
	C Controller module	Q06CCPU-V, Q06CCPU-V-B, Q12DCCPU-V, Q24DHCCPU-V, Q24DHCCPU-VG, Q24DHCCPU-LS, Q26DHCCPU-LS	○	○	×	○
	PC CPU module		○	○	×	○
Reference			Page 138, Section 6.1.2, Page 153, Section 6.1.3	Page 162, Section 6.1.4	Page 163, Section 6.2	Page 165, Section 6.3

*1 There are restrictions on available instructions depending on the version of the Motion CPU used. (Manual for the Motion CPU used)

6.1 Communications Using the CPU Shared Memory

This section describes data communications among CPU modules in a multiple CPU system using the CPU shared memory.

(1) CPU shared memory

The CPU shared memory is a data storage area in a CPU module and used to read/write data among CPU modules in a multiple CPU system.

The CPU shared memory consists of the areas listed below.

Area		Description	Reference
Host CPU operation information area		An area used to store error information and LED status of the CPU module	Page 122, Section 6.1 (2), Page 124, Section 6.1 (3)
System area		An area used by the operating system of the CPU module	–
Auto refresh area		An area used to communicate data by auto refresh. This area starts from the next address of the last address in the system area.	Page 122, Section 6.1 (2), Page 125, Section 6.1.1
User setting area		An area used to communicate data by a program. This area is assigned to the later addresses of those used for the auto refresh area. If auto refresh is not performed, the area starts from the next address of the last address in the system area.	Page 122, Section 6.1 (2), Page 153, Section 6.1.3
Multiple CPU high speed transmission area		An area to communicate data with other CPU modules in the multiple CPU system using Universal model QCPUs (except the Q00UCPU, Q01UCPU, and Q02UCPU)	Page 122, Section 6.1 (2)
	User setting area	An area used to communicate data by a program. This area is assigned to the address 10000_H and later of the CPU shared memory.	Page 153, Section 6.1.3
	Auto refresh area	An area used to communicate data by auto refresh	Page 138, Section 6.1.2

Point

Use of the multiple CPU high speed transmission area enables high-speed transmission by reducing the increase in scan time. Some conditions apply to using the area.

- Data communications by auto refresh: Page 138, Section 6.1.2
- Data communications by programs: Page 153, Section 6.1.3

(2) CPU shared memory configuration and availability of data communications by programs

The following shows the CPU shared memory configuration and the availability of data communications by programs using the CPU shared memory.

- Basic model QCPU

CPU shared memory		Host CPU		Other CPUs	
		Write	Read	Write	Read
(0H) 0 to (5FH) 95	Host CPU operation information area	×	○	×	○
(60H) 96 to (BFH) 191	System area	×	×	×	○ *1
(C0H) 192 to (1FFH) 511	Auto refresh area	×	×	×	×
	User setting area	○	○	×	○

○: Communications available, ×: Communications not available

*1 The system area is used to communicate data using motion dedicated instructions. For applications and uses of the system area, refer to the programming manual for the Motion CPU used.

- High Performance model QCPU and Process CPU

CPU shared memory		Host CPU		Other CPUs	
		Write	Read	Write	Read
(0H) 0 to (1FFH) 511	Host CPU operation information area	×	×	×	○
(200H) 512 to (7FFH) 2047	System area	×	×	×	○ *1
(800H) 2048 to (FFFH) 4095	Auto refresh area	×	×	×	×
	User setting area	○	×	×	○

○: Communications available, ×: Communications not available

*1 The system area is used to communicate data using motion dedicated instructions. For applications and uses of the system area, refer to the programming manual for the Motion CPU used.

• Universal model QCPU

		CPU shared memory	Host CPU		Other CPU	
			Write	Read	Write	Read
(0H) to (1FFH)	G0 to G511	Host CPU operation information area	×	○	×	○
(200H) to (7FFH)	G512 to G2047	System area	×	×	×	○
(800H) to (FFFH)	G2048 to G4095	Auto refresh area	×	×	×	×
		User setting area	○	○	×	○
(1000H) to (270FH)	G4096 to G9999	Use-prohibited area*1	×	×	×	×
(2710H) to (5F0FH)	G10000 to Max. G24335	Multiple CPU high speed transmission area*1	○	○	×	○

○: Communications available, ×: Communications not available

*1 The Q00UCPU, Q01UCPU, and Q02UCPU do not have the use-prohibited area and the multiple CPU high speed transmission area.

(3) Host CPU operation information area

(a) Information stored

The following information about the host CPU module is stored in this area.[*1]
In a single CPU system, all the values are set to 0.

Shared memory address	Name	Meaning	Description[*2]	Corresponding special register
0_H	Information existence	Information existence flag	This is an area to check whether information is stored in the host CPU operation information area (1_H to $1F_H$). • 0: Information not stored • 1: Information stored	–
1_H	Diagnostic error	Diagnostic error code	The error code of an error detected by the diagnostics is stored in binary.	SD0
2_H	Clock time for diagnosis error occurrence	Clock time for diagnosis error occurrence	The year and month when the error code was stored in the CPU shared memory (address: 1_H) are stored in 2-digit BCD.	SD1
3_H			The day and hour when the error code was stored in the CPU shared memory (address: 1_H) are stored in 2-digit BCD.	SD2
4_H			The minute and second when the error code was stored in the CPU shared memory (address: 1_H) are stored in 2-digit BCD.	SD3
5_H	Error information category code	Error information category code	A category code indicating an error information type (error common information or error individual information) is stored.	SD4
6_H to 10_H	Error common information	Error common information	The common information corresponding to the error code is stored.	SD5 to SD15
11_H to $1B_H$	Error individual information	Error individual information	The individual information corresponding to the error code is stored.	SD16 to SD26
$1C_H$	Not used	–	Use prohibited	–
$1D_H$	Switch status	Switch status of a CPU module	The switch status of the CPU module is stored.	SD200
$1E_H$	LED status	LED status of a CPU module	The LED status of the CPU module is stored.	SD201
$1F_H$	CPU operating status	Operating status of a CPU module	The operating status of the CPU module is stored.	SD203

*1 Motion CPUs do not use the areas 5_H to $1C_H$.
If data in the areas 5_H to $1C_H$ are read from a Motion CPU, the data will be read as "0".

*2 For details, refer to the description of the corresponding special register areas in the QCPU User's Manual (Hardware Design, Maintenance and Inspection).

(b) Reading data

Other QCPUs in the multiple CPU system can read data in the host CPU operation information area by executing the FROM instruction or the instructions using the cyclic transmission area device (U3En\G□).
Use the read data for monitoring purposes only because there is a delay in updating data.

6.1.1 Communications by auto refresh (using the auto refresh area)

This section describes data communications by auto refresh using the auto refresh area in the CPU shared memory.

Point

Data communications by auto refresh can also be performed using the auto refresh area in the multiple CPU high speed transmission area. Use of the multiple CPU high speed transmission area can reduce the increase in scan time. Some conditions apply to using the area. (Page 138, Section 6.1.2)

(1) Communications by auto refresh

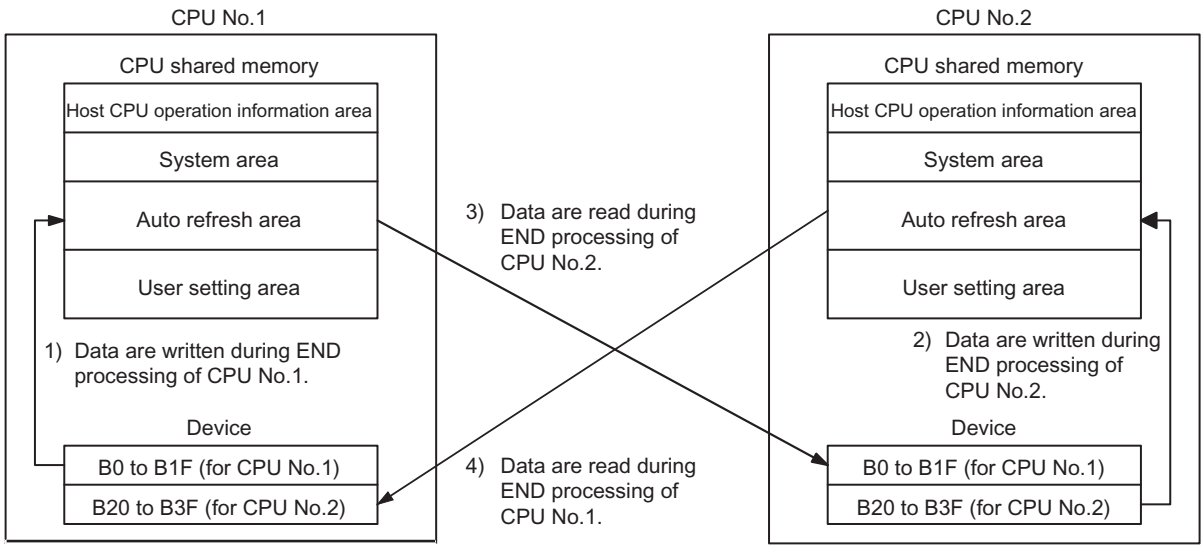
(a) Overview

Auto refresh communicates data using the auto refresh area in the CPU shared memory. Data are automatically read/written among all the CPU modules in the multiple CPU system by setting "Communication Area Setting (Refresh Setting)" in PLC parameter ("Multiple CPU Setting").
Since auto refresh automatically reads device data in other CPU modules, the host CPU module can use those device data.

Point

Auto refresh increases the scan time in the multiple CPU system. (Page 195, Appendix 4)

Ex. Operations when CPU No.1 performs auto refresh of data in B0 to B1F (32 points) and CPU No.2 performs auto refresh of data in B20 to B3F (32 points)



- Processing performed during END processing of CPU No.1
  1) CPU No.1 transfers the device data (B0 to B1F) to the auto refresh area in its own CPU shared memory.
  4) CPU No.1 reads the data in the auto refresh area of the CPU No.2's CPU shared memory and stores them in B20 to B3F of its own.
- Processing performed during END processing of CPU No.2
  2) CPU No.2 transfers the device data (B20 to B3F) to the auto refresh area in its own CPU shared memory.
  3) CPU No.2 reads the data in the auto refresh area of the CPU No.1's CPU shared memory and stores them in B0 to B1F of its own.

(b) Executing auto refresh

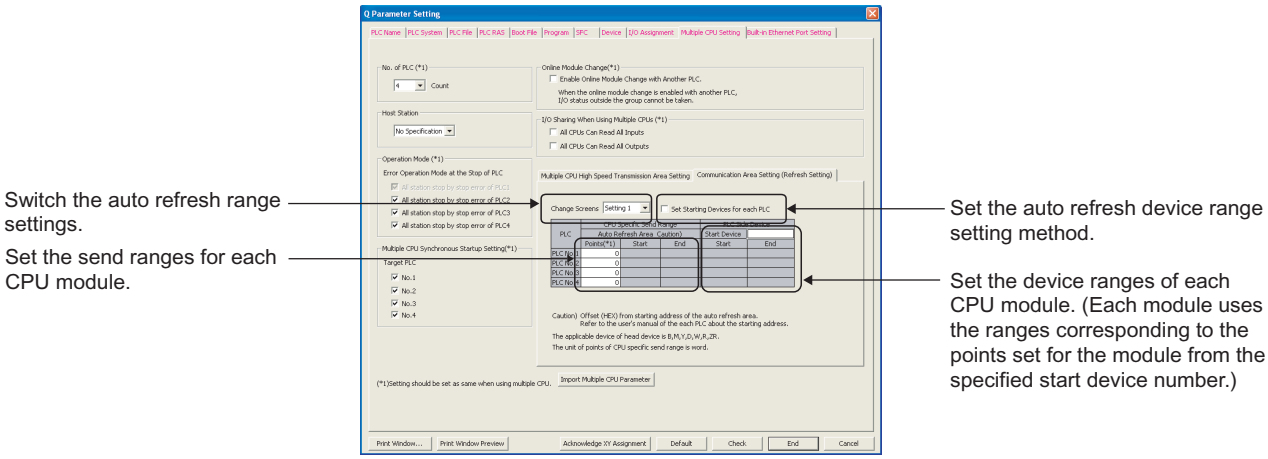
Auto refresh is executed when the CPU modules are in RUN, STOP, or PAUSE status. Auto refresh cannot be executed when a stop error has occurred in any of the CPU modules.

If a stop error occurs in a CPU module, the other modules will hold the data prior to the stop error. In the figure on Page 125, Section 6.1.1 (1) (a), for example, if the status of B20 is on when a stop error occurs in CPU No.2, the B20 in CPU No.1 will remain on.

(2) Auto refresh settings

To communicate data by auto refresh, set the ranges (number of points) to be sent by each CPU module ("CPU Specific Send Range") and the devices for storing data ("PLC Side Device") in PLC parameter ("Multiple CPU Setting").

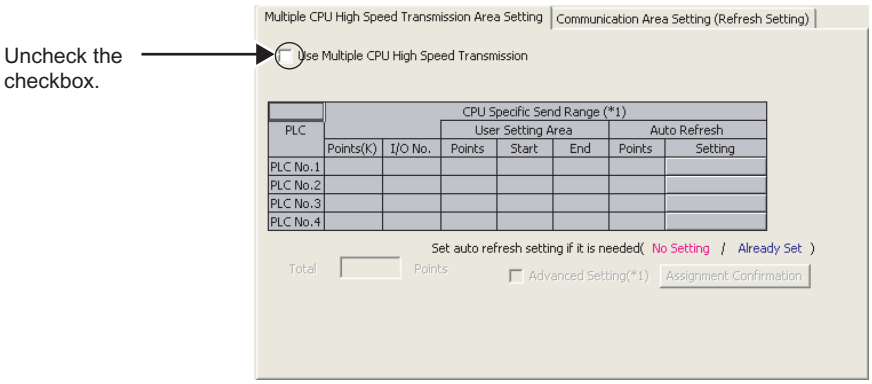
Project window ⇨ [Parameter] ⇨ [PLC Parameter] ⇨ [Multiple CPU Setting] ⇨ "Communication Area Setting (Refresh Setting)"



Point

In the following cases, uncheck the "Use Multiple CPU High Speed Transmission" checkbox in the "Multiple High Speed Transmission Area setting" area set for the Universal model QCPU.

- A High Performance model QCPU or Process CPU is used as CPU No.1.
- The "Use Multiple CPU High Speed Transmission" checkbox is unchecked for the Universal model QCPU used as CPU No.1.
- A main base unit, slim type main base unit, or redundant power main base unit is used.



(a) "Change Screens"

Up to four auto refresh ranges can be set. Set and switch the ranges in this parameter. With different settings, on/off data in bit devices and other data in word devices can be auto-refreshed separately.

(b) "CPU Specific Send Range"

Set the number of points in the CPU shared memory in increments of two points (two words). (If a bit device is specified in "PLC Side Device", two points equal to 32 points.)
If the number of points is set to "0", the data of the corresponding CPU module is not refreshed.

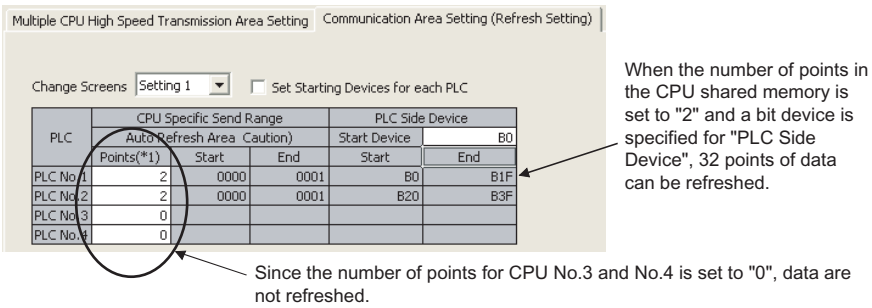
The following number of send points can be set for each CPU module.

QCPU	Number of send points
Basic model QCPU	• Basic model QCPU: 320 words • Motion CPU, C Controller module, PC CPU module: 2048 words • All CPU modules in total: 4416 points (4416 words)
High Performance model QCPU, Process CPU, Universal model QCPU	• Total of four ranges per CPU module: Up to 2K words • All CPU modules in total: 8K points (8K words)

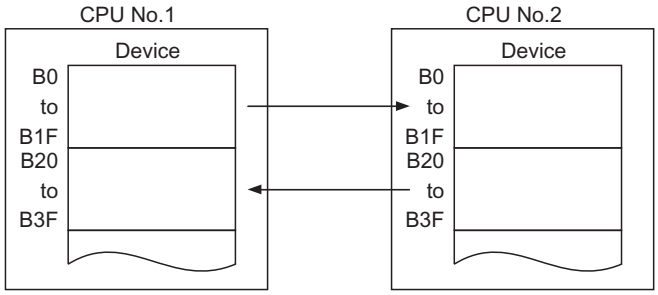
Point

Set the same number of send points for all the CPU modules in the multiple CPU system. If not, "PARAMETER ERROR" will be detected in the consistency check.

Ex. To refresh data in B0 to B1F (32 points) of CPU No.1 and B20 to B3F (32 points) of CPU No.2, set "2" in "Points" because the link relay (B) is a bit device.

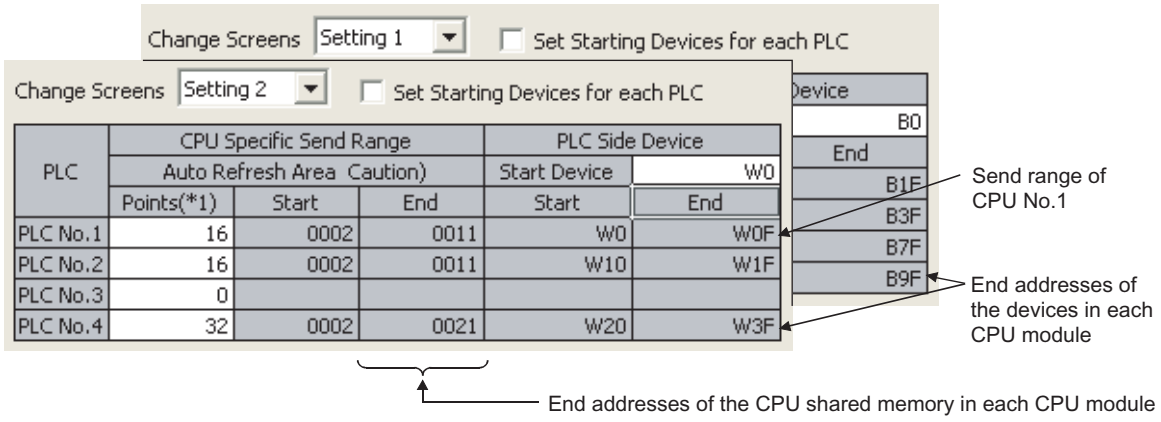


[Auto refresh processing]



The auto refresh area in the CPU shared memory occupies a total points set for Setting 1 to 4.
When the number of send points is set, the corresponding start and end addresses of the auto refresh area are automatically displayed in hexadecimal offset values.

Ex. For the CPU module having two auto refresh area settings (Setting 1 and 2), the end address of the auto refresh area will be the one "start address of the auto refresh area + offset value of Setting 2". In the following example, CPU No.1 and No.2 use the area from the start address of the auto refresh area to 0011_H, and CPU No.4 uses the area from the start address of the auto refresh area to 0021_H.
For the CPU module having only one auto refresh area setting (Setting 1), the end address of the auto refresh area will be the one set in Setting 1. In the following example, CPU No.3 uses only the area set in Setting 1.



(c) "PLC Side Device"

Set auto refresh target devices. The following devices can be set.

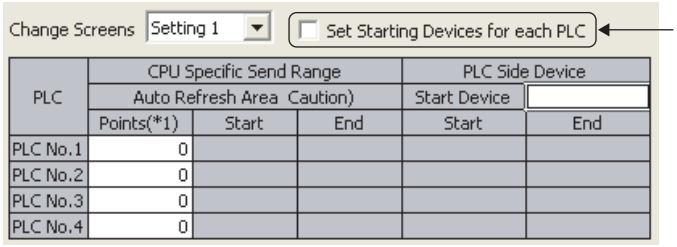
Device	Restriction
Data register (D), Link register (W), File register (R, ZR)	–
Link relay (B), Internal relay (M), Output (Y)	Specify 0 or multiples of 16 for the start number.

There are two auto refresh device range setting methods.*1

- Setting device ranges sequentially from the start device number of CPU No.1
- Setting device ranges for each CPU module freely

*1 Auto refresh devices of the following QCPUs can only be set sequentially from the start device of CPU No.1.
- Basic model QCPU
- High Performance model QCPU with a serial number (first five digits) of "07031" or earlier
- Process CPU

In addition, when GX Developer version 8.22Y or earlier is used, auto refresh devices shall only be set sequentially from the start device of CPU No.1.



Each CPU module uses the device ranges corresponding to the points set for the module from the specified start device number as the auto refresh target ranges. Set device numbers so that the necessary amount of send points can be secured.

- Different devices can be set for Setting 1 to 4.
  The same device can also be set as long as the device ranges for Setting 1 to 4 are not overlapped.

Setting 1: The link relay (B) is specified.

Change Screens: Setting 1 — Set Starting Devices for each PLC

PLC	CPU Specific Send Range			PLC Side Device	
	Auto Refresh Area Caution)			Start Device	B0
	Points(*1)	Start	End	Start	End
PLC No.1	2	0000	0001	B0	B1F
PLC No.2	2	0000	0001	B20	B3F
PLC No.3	4	0000	0003	B40	B7F
PLC No.4	2	0000	0001	B80	B9F

Setting 2: The link register (W) is specified.

Change Screens: Setting 2 — Set Starting Devices for each PLC

PLC	CPU Specific Send Range			PLC Side Device	
	Auto Refresh Area Caution)			Start Device	W0
	Points(*1)	Start	End	Start	End
PLC No.1	16	0002	0011	W0	W0F
PLC No.2	16	0002	0011	W10	W1F
PLC No.3	0				
PLC No.4	32	0002	0021	W20	W3F

Setting 3: The link relay (B) is specified.

Change Screens: Setting 3 — Set Starting Devices for each PLC

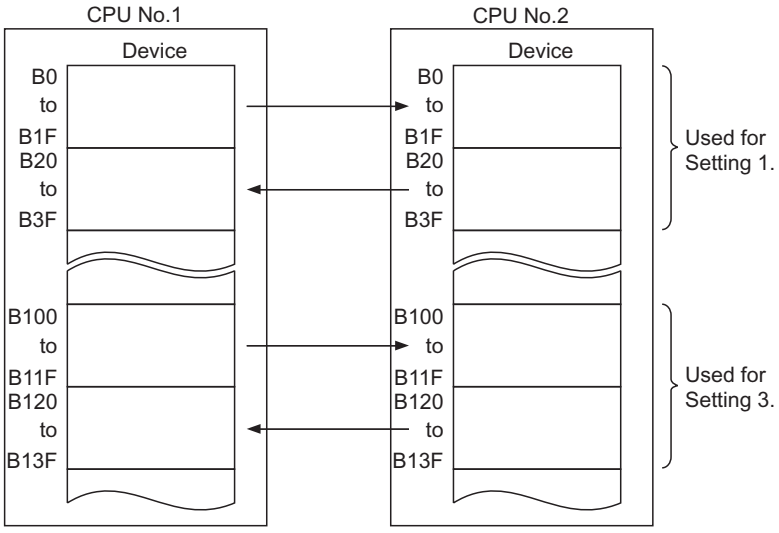
PLC	CPU Specific Send Range			PLC Side Device	
	Auto Refresh Area Caution)			Start Device	B100
	Points(*1)	Start	End	Start	End
PLC No.1	2	0012	0013	B100	B11F
PLC No.2	2	0012	0013	B120	B13F
PLC No.3	4	0004	0007	B140	B17F
PLC No.4	4	0022	0025	B180	B1BF

Different devices can be set for Setting 1 to 4.

The same device can also be set for Setting 1 to 4. Make sure the device ranges are not overlapped. In the setting example here, since the link relay ranges B0 to B9F (160 points) are used for Setting 1, set the link relay ranges BA0 and later for Setting 3.

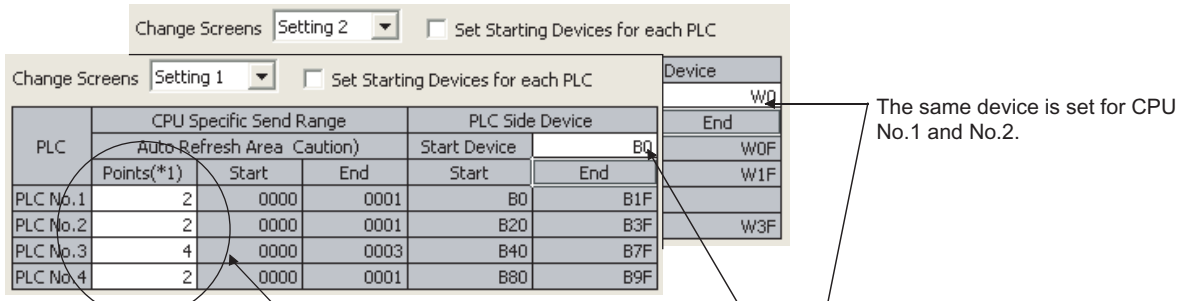
The start and end addresses are automatically calculated by the programming tool.

[Auto refresh processing]



- Devices of Setting 1 to 4 can be set independently for each CPU module.
  For example, while the link relay (B) is set for CPU No.1, the internal relay (M) can be set for CPU No.2.

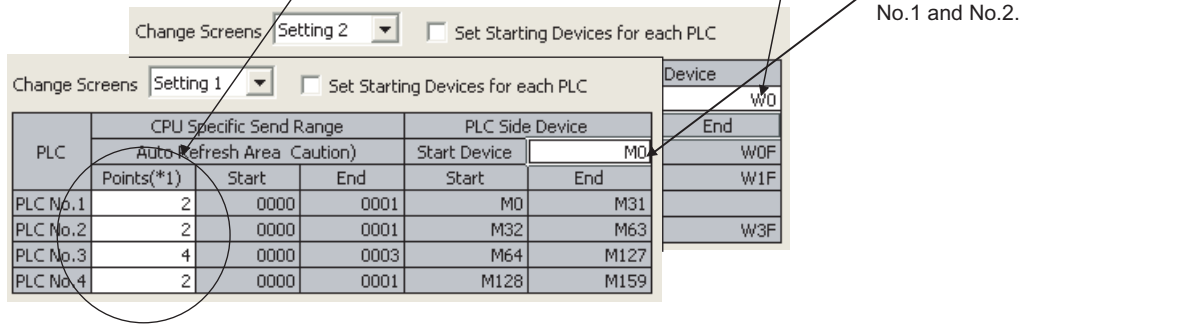
Refresh setting of CPU No.1



The same device is set for CPU No.1 and No.2.

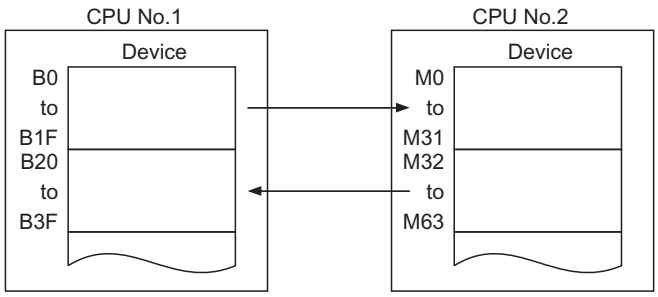
The same number of points is set for all the CPU modules.

Refresh setting of CPU No.2

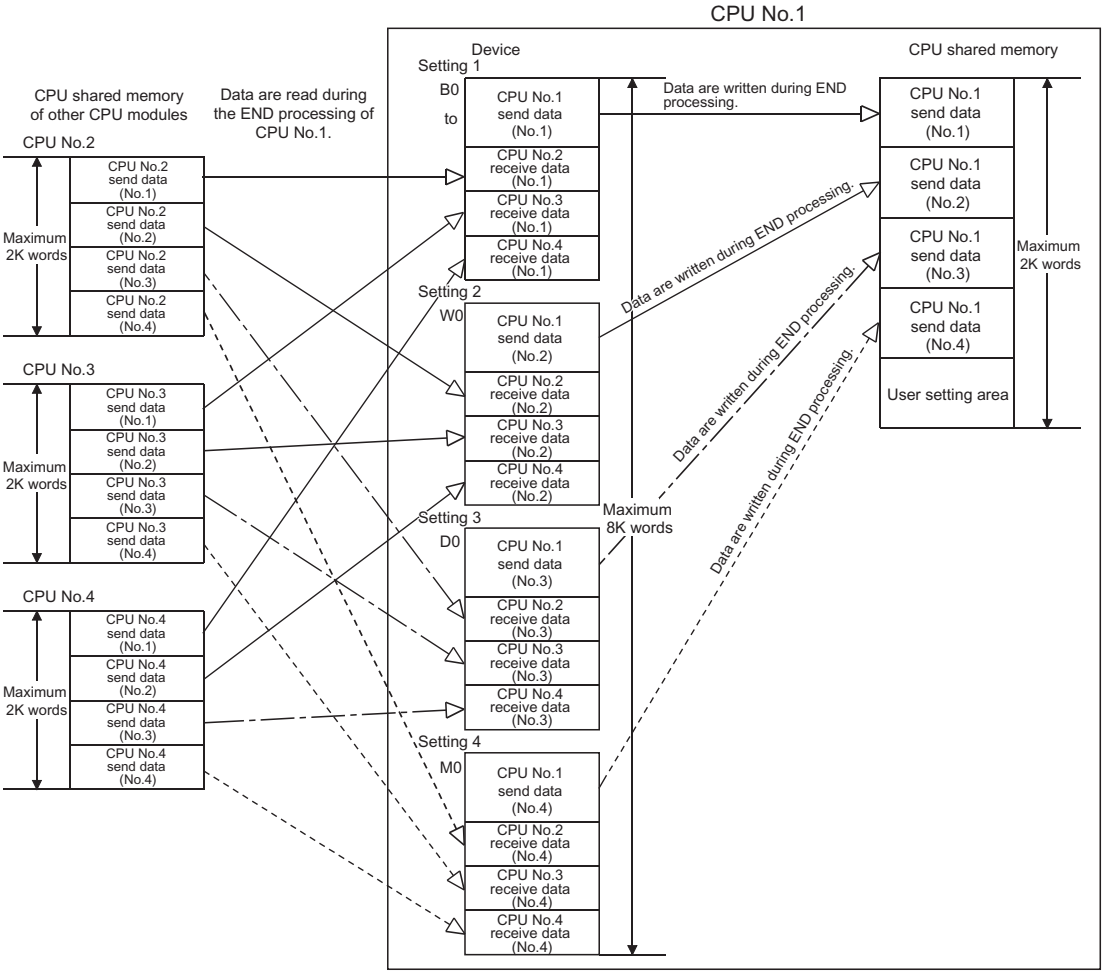


Different devices are set for CPU No.1 and No.2.

[Auto refresh processing]



Ex. Operations when executing auto refresh of four ranges (Setting 1: link relay (B), Setting 2: link register (W), Setting 3: data register (D), Setting 4: internal relay (M))



- There are following advantages if device ranges are set for each CPU module freely.
  - The order of the send ranges can be changed for each CPU module.
  - Since unnecessary refresh can set to be disabled, the system scan time will be reduced.

Ex. Changing the order of send ranges for each CPU module

The following is a setting example of auto refresh between the High Performance model QCPU used as CPU No.1 and the Motion CPU used as CPU No.2. By setting the device ranges freely, the device in the High Performance model QCPU can be matched to the that in the Motion CPU.

Change Screens: Setting 1 — Set Starting Devices for each PLC

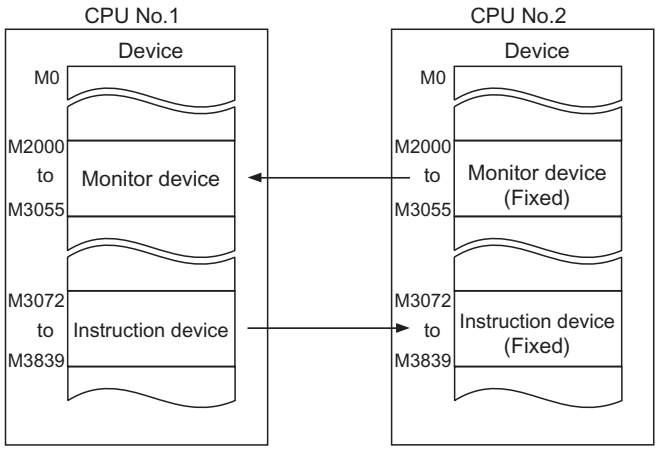
PLC	CPU Specific Send Range			PLC Side Device	
	Auto Refresh Area Caution)			Start Device	
	Points(*1)	Start	End	Start	End
PLC No.1	48	0000	002F	M3072	M3839
PLC No.2	66	0000	0041	M2000	M3055
PLC No.3					
PLC No.4					

Setting of CPU No.1

Change Screens: Setting 1 — Set Starting Devices for each PLC

PLC	CPU Specific Send Range			PLC Side Device	
	Auto Refresh Area Caution)			Start Device	
	Points(*1)	Start	End	Start	End
PLC No.1	48	0000	002F	M3072	M3839
PLC No.2	66	0000	0041	M2000	M3055
PLC No.3					
PLC No.4					

Setting of CPU No.2



Ex. Disabling unnecessary refresh

Unnecessary refresh can set to be disabled by not setting the device ranges of other CPU modules where auto refresh is not required. The device ranges of the host CPU module must be set.

The following is a setting example of auto refresh between CPU No.1 and each of other CPU modules (CPU No.2 to No.4).

Change Screens: Setting 1 ☑ Set Starting Devices for each PLC

PLC	CPU Specific Send Range			PLC Side Device	
	Auto Refresh Area Caution)			Start Device	
	Points(*1)	Start	End	Start	End
PLC No.1	10	0000	0009	D100	D109
PLC No.2	10	0000	0009	D0	D9
PLC No.3	10	0000	0009	D10	D19
PLC No.4	10	0000	0009	D20	D29

Setting of CPU No.1

Change Screens: Setting 1 ☑ Set Starting Devices for each PLC

PLC	CPU Specific Send Range			PLC Side Device	
	Auto Refresh Area Caution)			Start Device	
	Points(*1)	Start	End	Start	End
PLC No.1	10	0000	0009	D100	D109
PLC No.2	10	0000	0009	D0	D9
PLC No.3	10	0000	0009		
PLC No.4	10	0000	0009		

Setting of CPU No.2

Change Screens: Setting 1 ☑ Set Starting Devices for each PLC

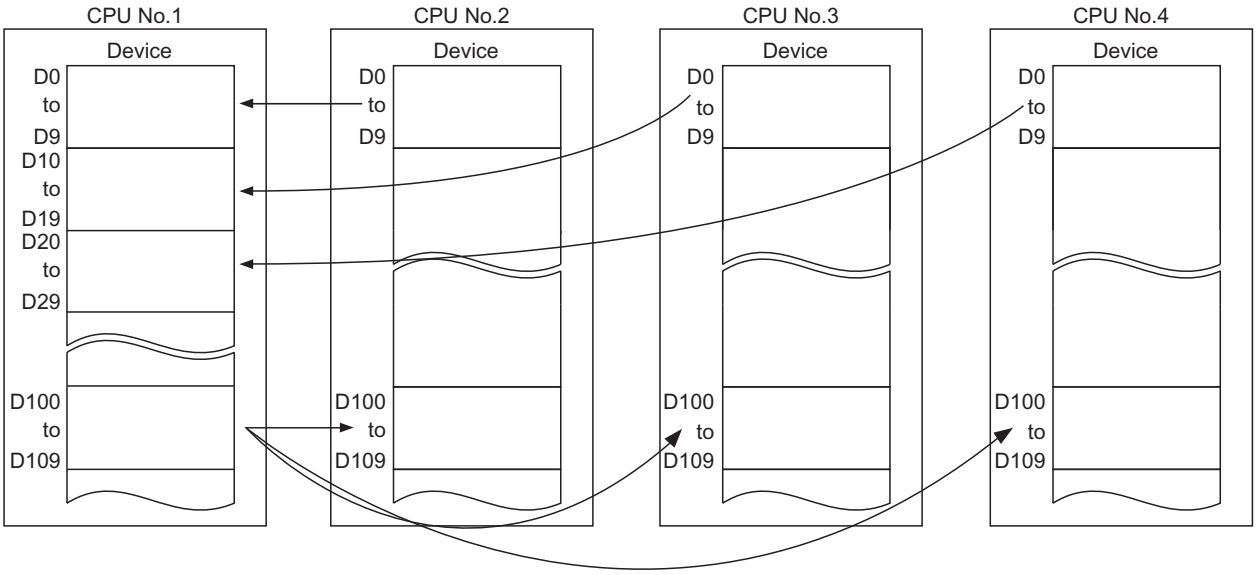
PLC	CPU Specific Send Range			PLC Side Device	
	Auto Refresh Area Caution)			Start Device	
	Points(*1)	Start	End	Start	End
PLC No.1	10	0000	0009	D100	D109
PLC No.2	10	0000	0009		
PLC No.3	10	0000	0009	D0	D9
PLC No.4	10	0000	0009		

Setting of CPU No.3

Change Screens: Setting 1 ☑ Set Starting Devices for each PLC

PLC	CPU Specific Send Range			PLC Side Device	
	Auto Refresh Area Caution)			Start Device	
	Points(*1)	Start	End	Start	End
PLC No.1	10	0000	0009	D100	D109
PLC No.2	10	0000	0009		
PLC No.3	10	0000	0009		
PLC No.4	10	0000	0009	D0	D9

Setting of CPU No.4



(3) Precautions

(a) Local device setting (except the Basic model QCPU)

Device ranges set for the auto refresh target cannot be set as local devices. If set, the refresh data will not be updated.

(b) Using the same file name as that of the program in the file register (except the Basic model QCPU)

Do not set the file register of each program as an auto refresh target device. If set, data are automatically refreshed to the file register corresponding to the scan execution type program executed last.

(c) Assurance of send data

Old data and new data may coexist (data inconsistency) in each CPU module due to the timing of refreshing data in the host CPU module and reading data in other CPU modules.
The following are the methods to prevent data inconsistency in data communications by auto refresh.

- Preventing inconsistency of 32-bit data
  Data inconsistency will not occur because the data transmission by auto refresh is performed only in units of 32 bits (parameters are set in increments of 32 bits).

- Preventing inconsistency of data exceeding 32 bits
  With auto refresh, data are read in descending order of the setting number in auto refresh setting parameter. To prevent data inconsistency, use the setting number lower than the setting data as an interlock device.

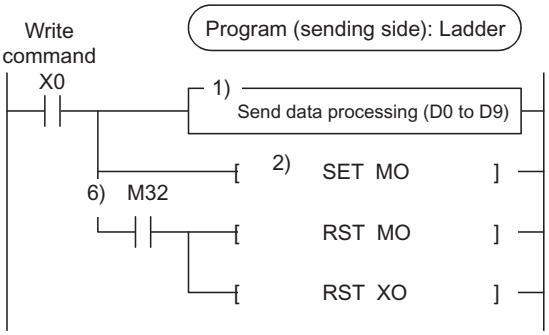
Ex. Auto refresh between a QCPU and a Motion CPU

The following are the program examples for the Basic model QCPU and Motion CPU when PLC parameters ("Communication Area Setting (Refresh Setting)" of "Multiple CPU Setting") are set as shown below.

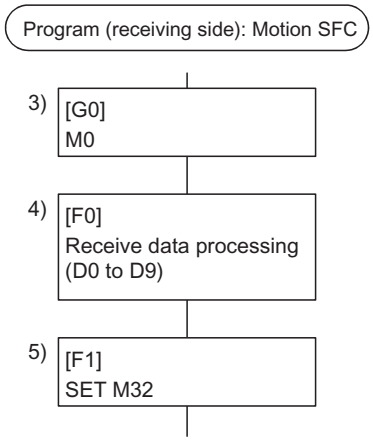
[Parameter setting]

Setting No. ("Change Screens")	PLC	CPU Specific Send Range			PLC Side Device	
		Points	Start	End	Start	End
Setting 1	PLC No.1	2	00C0	00C1	M0	M31
	PLC No.2	2	0800	0801	M32	M63
Setting 2	PLC No.1	10	00C2	00CB	D0	D9
	PLC No.2	0	–	–	–	–

Program example (sending side)



Program example (receiving side)



1) CPU No.1 creates send data.

2) CPU No.1 turns on the data setting complete bit.

(Auto refresh execution)

3) CPU No.2 detects the completion of send data setting.

4) CPU No.2 performs receive data processing.

5) CPU No.2 turns on the receive data processing complete bit.

(Auto refresh execution)

6) CPU No.1 detects the completion of the receive data processing, and turns off the data setting complete bit.

Ex. Auto refresh between QCPUs

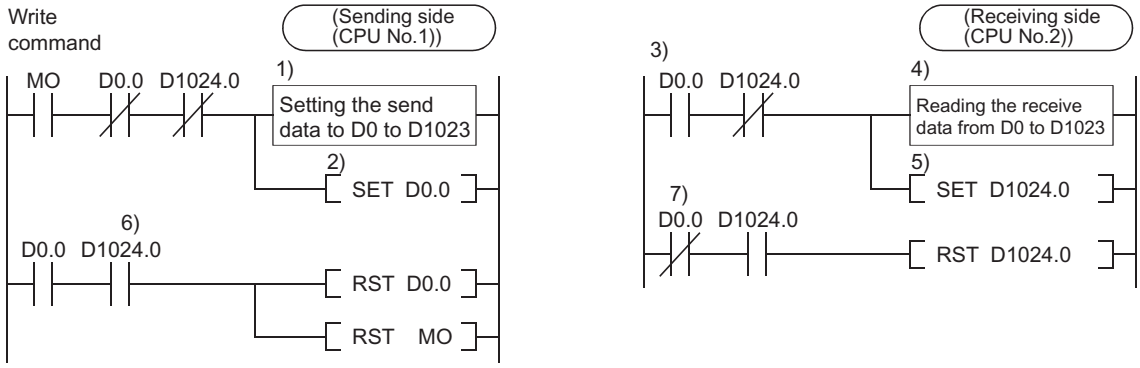
The following are the program examples for the High Performance model QCPUs when PLC parameters ("Communication Area Setting (Refresh Setting)" of "Multiple CPU Setting") are set as shown below.

[Parameter setting]

Setting No. ("Change Screens")	PLC	CPU Specific Send Range			PLC Side Device	
		Points	Start	End	Start	End
Setting 1	PLC No.1	1024	0000	03FF	D0	D1023
	PLC No.2	1024	0000	03FF	D1024	D2047

Use D0.0 as an interlock device of CPU No.1 (data setting complete bit) and D1024.0 as an interlock device of CPU No.2 (receive data processing complete bit).

Program example (sending side) (CPU No.1)Program example (receiving side) (CPU No.2)



1) CPU No.1 creates send data.
2) CPU No.1 turns on the data setting complete bit.

(Auto refresh execution)
3) CPU No.2 detects the completion of send data setting.
4) CPU No.2 performs receive data processing.
5) CPU No.2 turns on the receive data processing complete bit.

(Auto refresh execution)
6) CPU No.1 detects the completion of the receive data processing, and turns off the data setting complete bit.

(Auto refresh execution)
7) CPU No.2 detects the off status of the data setting complete bit, and turns off the receive data processing complete bit.

6.1.2 Communications by auto refresh (using the multiple CPU high speed transmission area)

This section describes data communications by auto refresh using the multiple CPU high speed transmission area in the CPU shared memory.

(1) Conditions for data communications

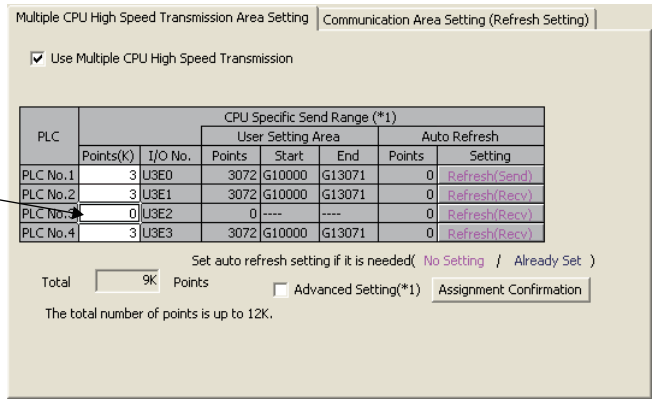
Data communications by auto refresh using the multiple CPU high speed transmission area can be performed only when the following conditions are all met.

- A multiple CPU high-speed main base unit (Q35DB, Q38DB, or Q312DB) is used.
- A Universal model QCPU (except the Q00UCPU, Q01UCPU, and Q02UCPU) is used as CPU No.1.
- At least two of the following CPU modules are used.
  - Universal model QCPU (except the Q00UCPU, Q01UCPU, and Q02UCPU)
  - Motion CPU (Q172DCPU(-S1), Q173DCPU(-S1), Q172DSCPU, or Q173DSCPU)
  - C Controller module (Q12DCCPU-V, Q24DHCCPU-V, Q24DHCCPU-VG, Q24DHCCPU-LS, or Q26DHCCPU-LS)

If any CPU module other than the above is mounted on the multiple CPU high-speed main base unit, set "0" to the auto refresh points ("Points") of the relevant CPU module in "Multiple CPU High Speed Transmission Area Setting" of PLC parameter.

Ex. Setting "0" to the auto refresh points of CPU No.3

Set "0" for the CPU module other than the Universal model QCPU (except the Q00UCPU, Q01UCPU, and Q02UCPU), Motion CPU (Q172DCPU(-S1), Q173DCPU(-S1), Q172DSCPU, or Q173DSCPU), and C Controller module (Q12DCCPU-V, Q24DHCCPU-V, Q24DHCCPU-VG, Q24DHCCPU-LS or Q26DHCCPU-LS).



Point

If all the conditions cannot be met, use the auto refresh area in the CPU shared memory. (Page 125, Section 6.1.1)

(2) Communications by auto refresh

(a) Overview

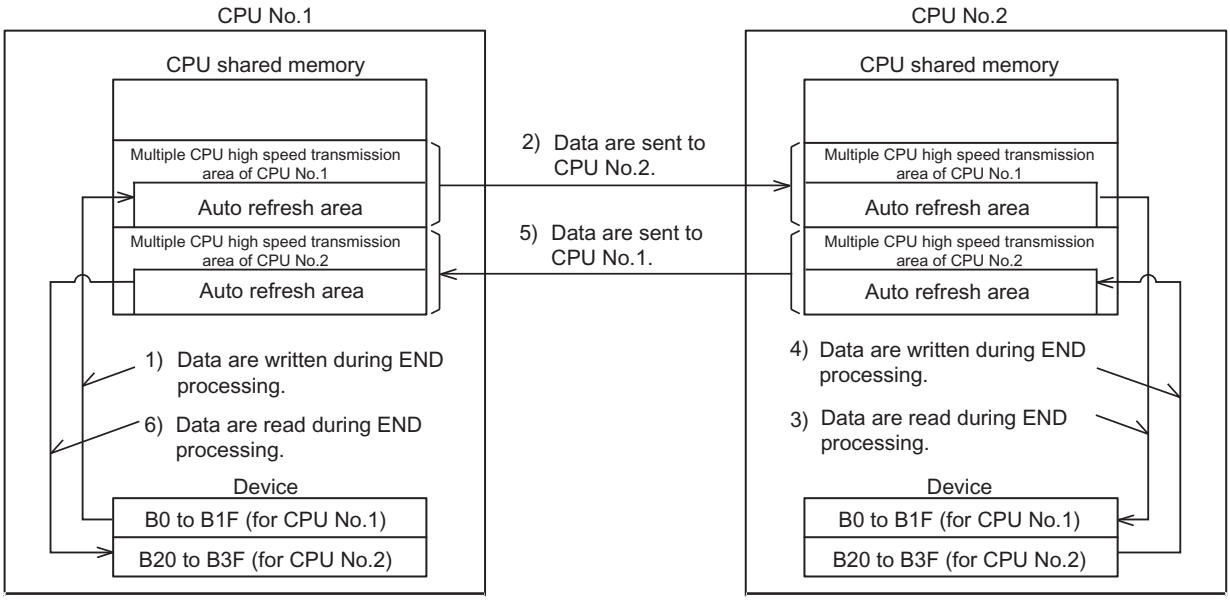
Auto refresh communicates data using the auto refresh area of the multiple CPU high speed transmission area in the CPU shared memory. The data written to the auto refresh area of the multiple CPU high speed transmission area is sent to that of the other CPU modules at regular intervals (multiple CPU high speed transmission cycles).

Data are automatically read/written among all the CPU modules in the multiple CPU system by setting "Multiple CPU High Speed Transmission Area Setting" in PLC parameter ("Multiple CPU Setting").
Since auto refresh automatically reads device data in other CPU modules, the host CPU module can use those device data.

Point

Auto refresh increases the scan time in the multiple CPU system. (Page 195, Appendix 4)

Ex. Operations when CPU No.1 performs auto refresh of data in B0 to B1F (32 points) and CPU No.2 performs auto refresh of data in B20 to B3F (32 points)

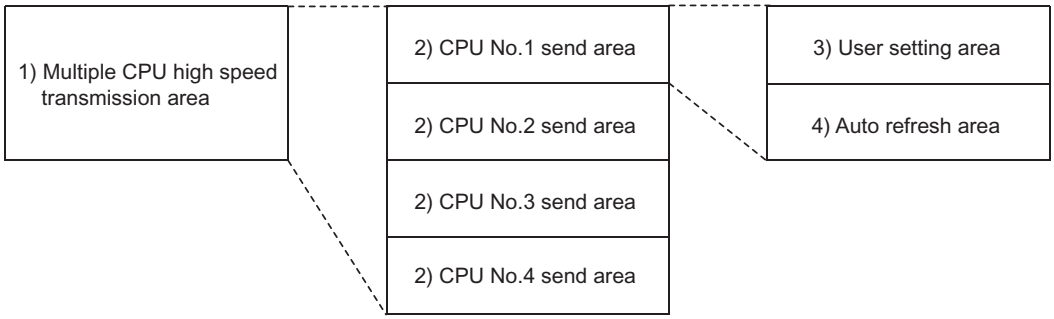


- Procedure for CPU No.2 to read device data of CPU No.1
  1) CPU No.1 transfers device data (B0 to B1F) to the auto refresh area in its own CPU shared memory during END processing.
  2) CPU No.1 sends the data in the multiple CPU high speed transmission area of its own to CPU No.2.
  3) CPU No.2 transfers the received data to B0 to B1F of its own during END processing.

- Procedure for CPU No.1 to read device data of CPU No.2
  4) CPU No.2 transfers device data (B20 to B3F) to the auto refresh area in its own CPU shared memory during END processing.
  5)CPU No.2 sends the data in the multiple CPU high speed transmission area of its own to CPU No.1.
  6) CPU No.1 transfers the received data to B20 to B3F of its own during END processing.

(b) Memory configuration of the multiple CPU high speed transmission area

The following shows the memory configuration of the multiple CPU high speed transmission area.
For the CPU shared memory configuration, refer to Page 121, Section 6.1.



No.	Name	Description	Size	
			Setting range	Setting unit
1)	Multiple CPU high speed transmission area	An area used to communicate data among CPU modules in the Multiple CPU system. The area up to 14K word is divided and assigned to CPU modules in the system.	0 to 14K words	1K word
2)	CPU No.n send area n (n=1 to 4)	An area used to store send data of each CPU module. Data sent to other CPU modules are stored in this area. Data received from other CPU modules are stored in the area as well.	0 to 14K words	1K word
3)	User setting area	An area used to communicate data with other CPU modules by executing instructions using the cyclic transmission area device	0 to 14K words	2 words
4)	Auto refresh area	An area to communicate data with other CPU modules by auto refresh	0 to 14K words	2 words

Point

When the COM instruction is used in the program, auto refresh is performed upon execution of the COM instruction. However, the scan time increases for the time required for the auto refresh. (MELSEC-Q/L Programming Manual (Common Instruction))

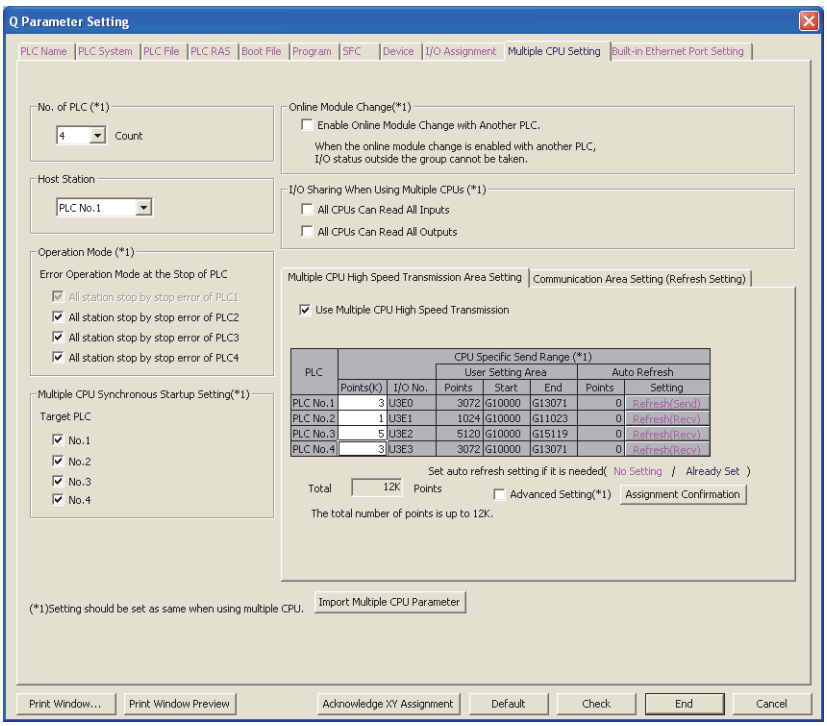
(c) Executing auto refresh

Auto refresh is executed when the CPU modules are in RUN, STOP, or PAUSE status. The auto refresh execution status when an error has occurred in any of the CPU modules differs depending on the error.
(Page 162, Section 6.1.4)

(3) Multiple CPU high speed transmission area settings

To perform auto refresh of data in the CPU shared memory, set the ranges (number of points) to be sent by each CPU module ("CPU Specific Send Range") and the devices for storing data ("Auto Refresh Setting") in PLC parameter ("Multiple CPU Setting").

Project window ⇨ [Parameter] ⇨ [PLC Parameter] ⇨ [Multiple CPU Setting] ⇨ "Multiple CPU High Speed Transmission Area Setting"

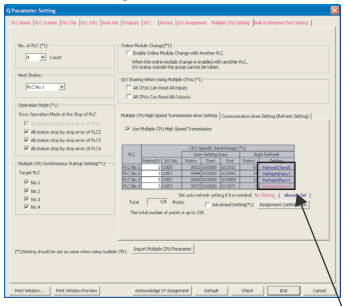


Point

To check the auto refresh directions, specify the CPU number in "Host Station" of PLC parameter ("Multiple CPU Setting").

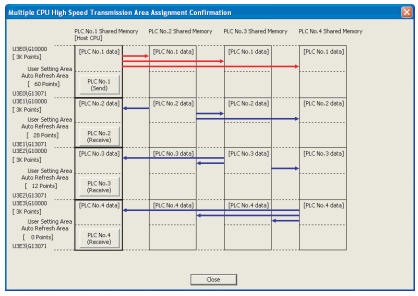
- Multiple CPU Setting window
- Auto Refresh Setting window
- Multiple CPU High Speed Transmission Area Assignment Confirmation window

Multiple CPU Setting window



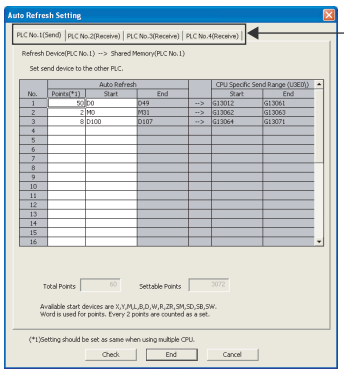
Click the Assignment Confirmation button.

Multiple CPU High Speed Transmission Area Assignment Confirmation window



Click the Refresh button.

Auto Refresh Setting window



The auto refresh directions can be checked.

Click the PLC No.1 (Send) button.

(a) "CPU Specific Send Range"

Set the number of points for the multiple CPU high speed transmission area used in each CPU module.

Item	Description	Setting/displayed range
CPU Specific Send Range	Set the number of send data points for each CPU module.*1 If a CPU module not listed on Page 138, Section 6.1.2 (1) is used, set "0" point to the corresponding CPU module.	Setting range: 0 to 14K points*2 Setting unit: 1K points
User Setting Area	The area used to communicate data with other CPU modules by programs is displayed. The number of points for this area is the number obtained by subtracting the points set for “Auto Refresh" from the points (K) set for "CPU Specific Send Range".	Displayed range: 0 to 14335 points
Auto Refresh	Set parameters required to communicate data with other CPU modules by auto refresh. The number of points set in the "Auto Refresh Setting" window is displayed. (Page 145, Section 6.1.2 (3) (b))	Displayed range: 0 to 14335 points

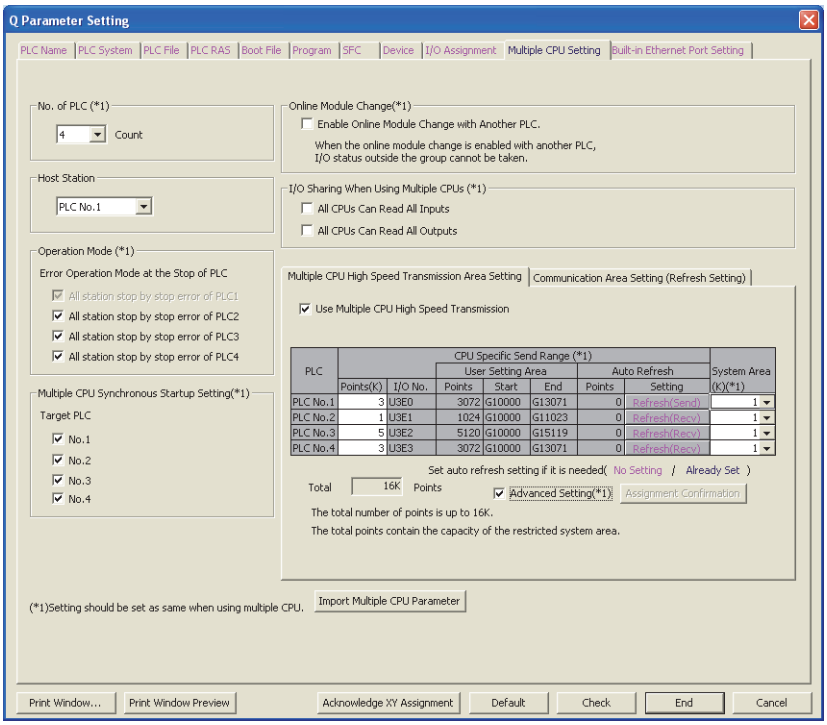
*1 The following number of points is set by default.

Number of CPU modules	Default of "CPU Specific Send Range"			
	CPU No.1	CPU No.2	CPU No.3	CPU No.4
2	7K points	7K points		
3	7K points	3K points	3K points	
4	3K points	3K points	3K points	3K points

*2 Set the number of points so that the total points of all the CPU modules will be the following points or less.
- When two CPU modules are mounted: 14K points
- When three CPU modules are mounted: 13K points
- When four CPU modules are mounted: 12K points

Point

The number of points for the system area used by dedicated instructions can be changed to 2K points by checking the "Advanced Setting" checkbox.
This increases the number of dedicated instructions can be executed simultaneously in one scan.



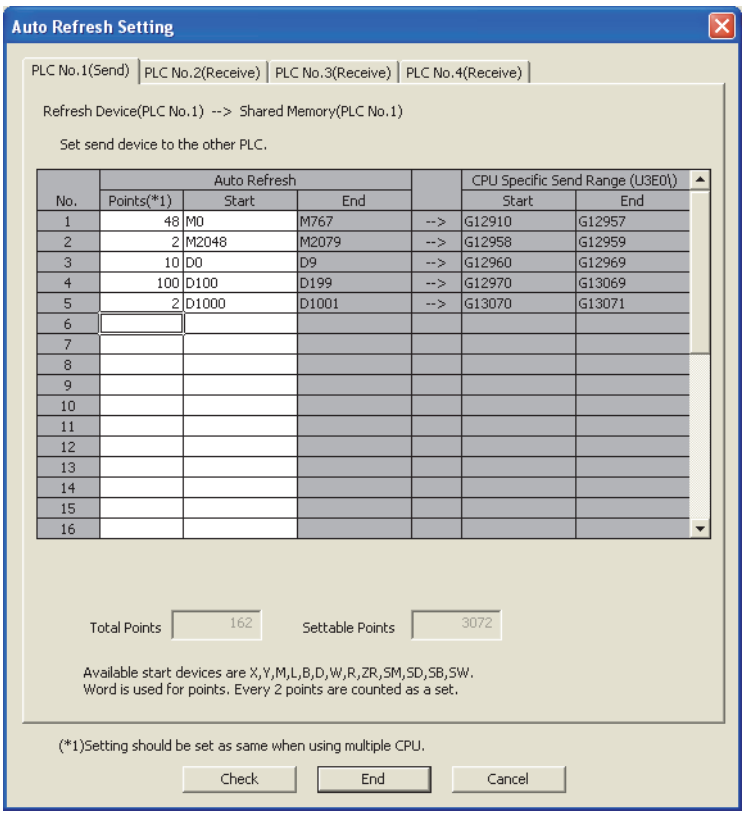
Item	Description	Setting/displayed range
CPU Specific Send Range	Set the number of send data points for each CPU module.	Setting range: 0 to 14K points*1 Setting unit: 1K points
System Area	The area used to communicate data by using motion dedicated instructions. (Manual for the Motion CPU used) Set the number of points for the system area used in each CPU module.	Setting range: 1K or 2K points
Total	The total of number of points set for the “CPU Specific Send Range" and "System Area" is displayed.	Displayed range: 1 to 16K points*2 Displayed unit: 1K points

*1 Set the number of points so that the total points of all the CPU modules will be the following points or less.
- When two CPU modules are mounted: 14K points
- When three CPU modules are mounted: 13K points
- When four CPU modules are mounted: 12K points

*2 Set the number of points so that the total points of all the CPU modules will be 16K points or less (including the points set for the system area).

(b) "Auto Refresh Setting"

Set auto refresh target devices to communicate data by auto refresh using the multiple CPU high speed transmission area. Up to 32 ranges can be set for each CPU module.



Item	Description	Setting range
Points	Set the number of points for data communications in increment of 2 points (word units).	• Setting range: 2 to 14336 points*1 • Setting unit: 2 points*2
Start	Specify the auto refresh target device. For the host CPU module, specify the send target device. For other CPU modules, specify the receive target device.	• Device that can send data*3 X, Y, M, L, B, D, W, R, ZR, SM, SD, SB, SW • Device that can receive data:*3 X, Y, M, L, B, D, W, R, ZR • Leave this field blank if auto refresh is not executed. (The field can be left blank only when it is used as a receive target device.)

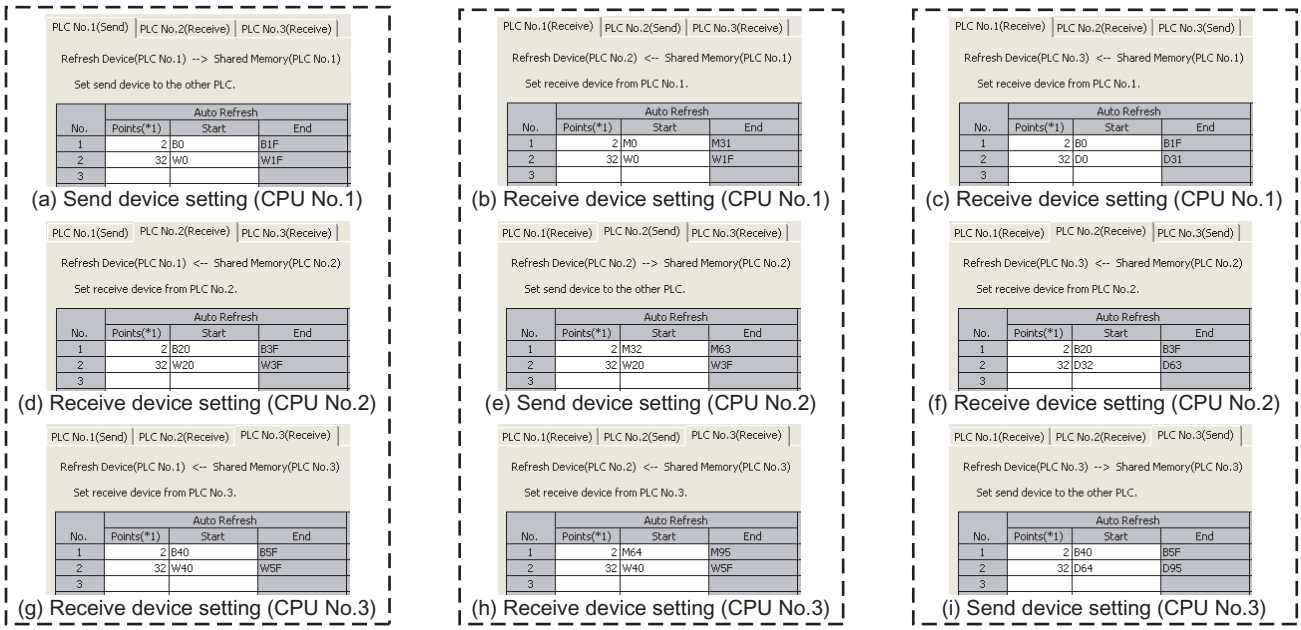
*1 Set the number of points within the points set for the "CPU Specific Send Range" of each CPU module.
*2 Bit devices can be specified in increments of 32 points (2 words).
*3 Set the device numbers for setting No.1 to No.32 so that they will not overlap.

(4) Auto refresh setting examples and data flow

The data flow among CPU modules will be as follows in a multiple CPU system containing three CPU modules with two auto refresh range settings.

(a) Auto refresh setting examples

The following are the examples of auto refresh settings to explain the data flow.

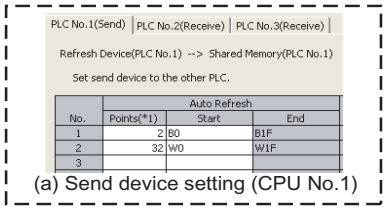


(1) Auto refresh setting of CPU No.1 (2) Auto refresh setting of CPU No.2 (3) Auto refresh setting of CPU No.3

(b) Flow of data sent from CPU No.1 to other CPU modules

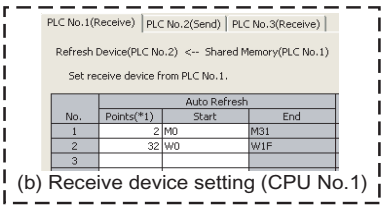
<Parameter setting>

Refer to those related to the data communications of CPU No.1 ((a) to (c)) among the auto refresh setting examples on Page 146, Section 6.1.2 (4) (a).



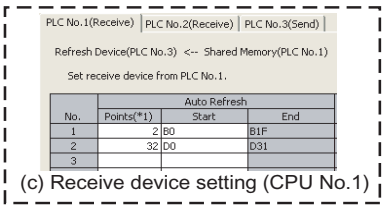
(a) Send device setting (CPU No.1)

(1) Auto refresh setting of CPU No.1



(b) Receive device setting (CPU No.1)

(2) Auto refresh setting of CPU No.2

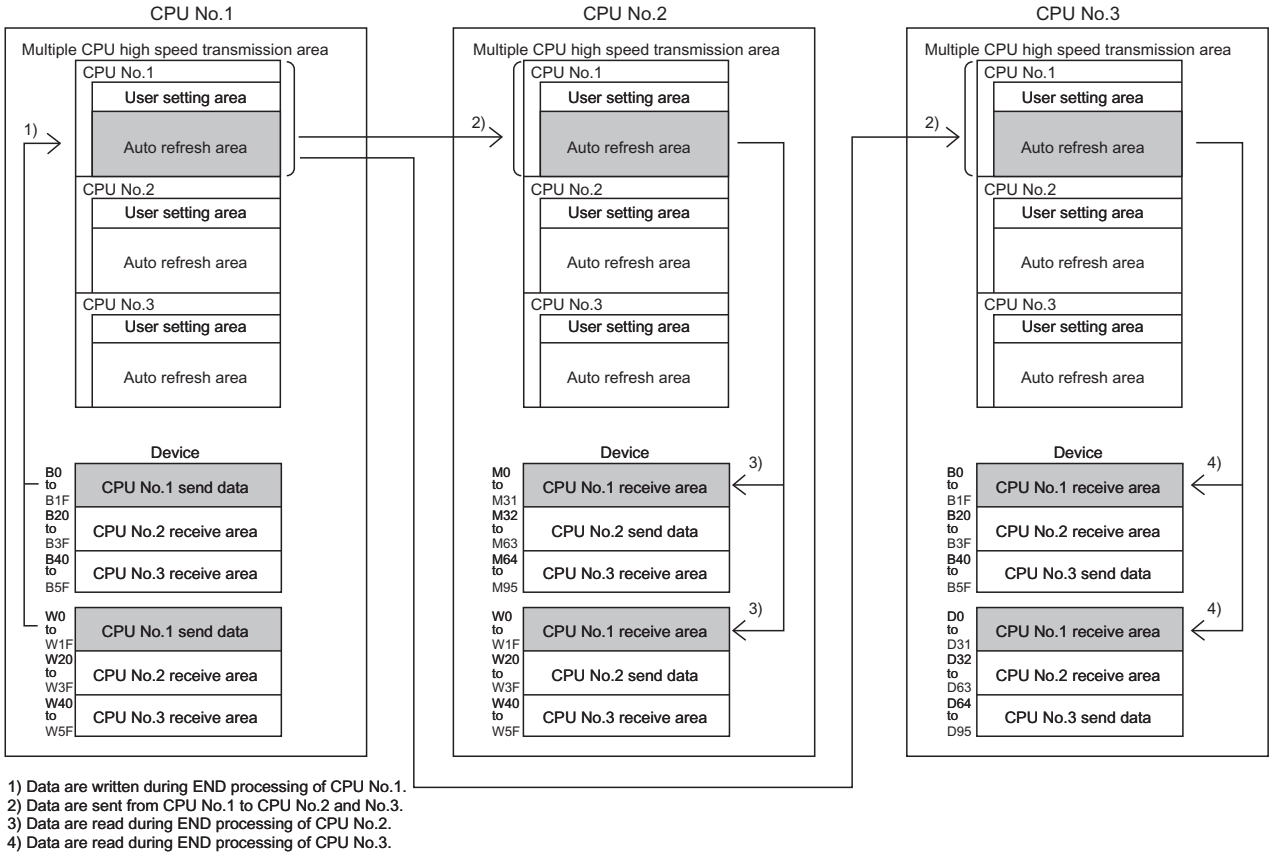


(c) Receive device setting (CPU No.1)

(3) Auto refresh setting of CPU No.3

<Flow of data sent from CPU No.1 to other CPU modules>

- CPU No.1 writes data (CPU No.1 send data) in the devices set in the auto refresh parameter to its own auto refresh area during END processing.
- CPU No.1 sends the data stored in its own auto refresh area to CPU No.2 and No.3 in each multiple CPU high speed transmission cycle.
- CPU No.2 and No.3 transfer the data received from CPU No.1 to the devices set in the auto refresh parameter (CPU No.1 receive area) during END processing.

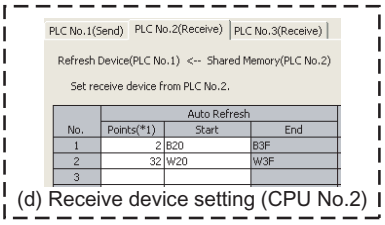


1) Data are written during END processing of CPU No.1.
2) Data are sent from CPU No.1 to CPU No.2 and No.3.
3) Data are read during END processing of CPU No.2.
4) Data are read during END processing of CPU No.3.

(c) Flow of data sent from CPU No.2 to other CPU modules

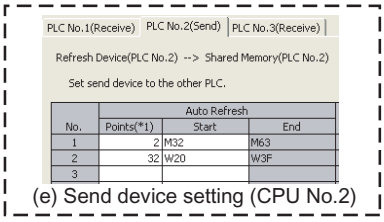
<Parameter setting>

Refer to those related to the data communications of CPU No.2 ((d) to (f)) among the auto refresh setting examples on Page 146, Section 6.1.2 (4) (a).



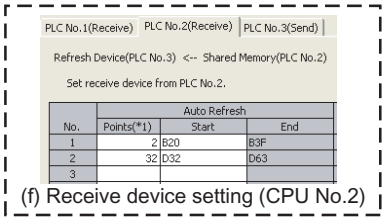
(d) Receive device setting (CPU No.2)

(1) Auto refresh setting of CPU No.1



(e) Send device setting (CPU No.2)

(2) Auto refresh setting of CPU No.2

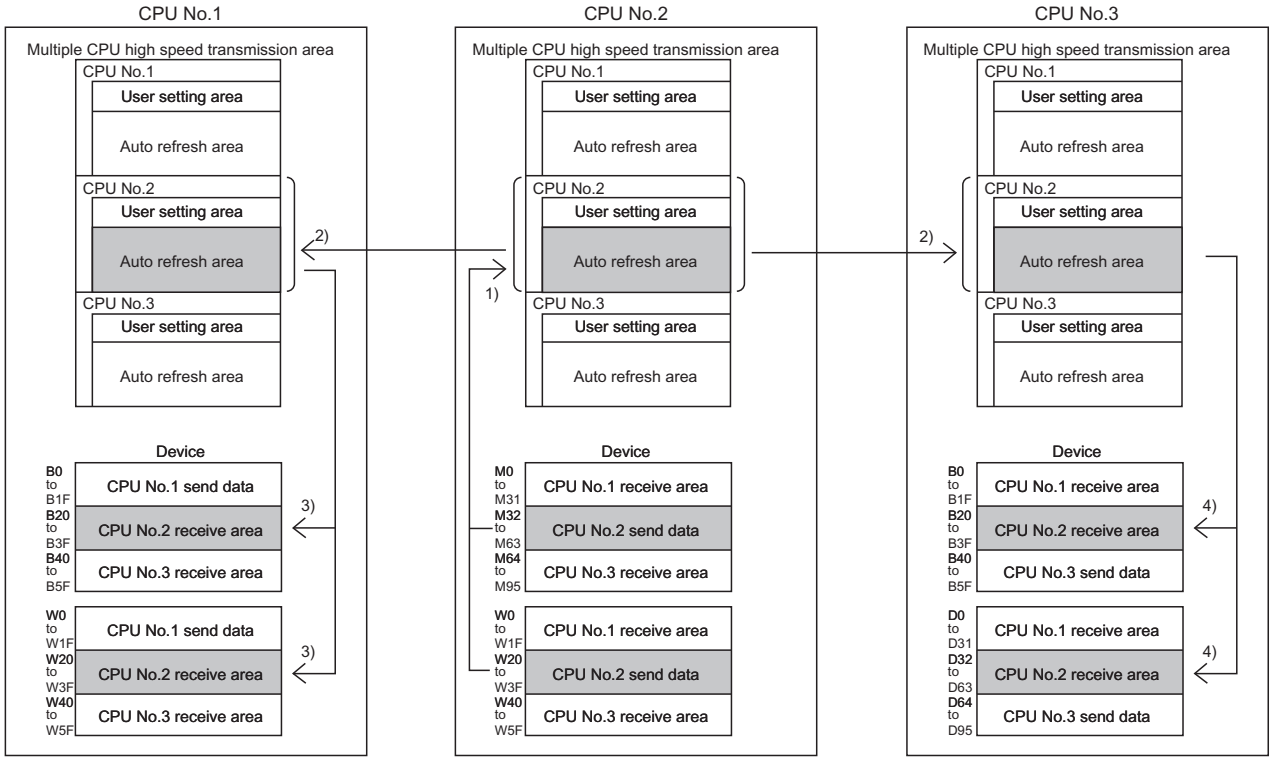


(f) Receive device setting (CPU No.2)

(3) Auto refresh setting of CPU No.3

<Flow of data sent from CPU No.2 to other CPU modules>

- CPU No.2 writes data (CPU No.2 send data) in the devices set in the auto refresh parameter to its own auto refresh area during END processing.
- CPU No.2 sends the data stored in its own auto refresh area to CPU No.1 and No.3 in each multiple CPU high speed transmission cycle.
- CPU No.1 and No.3 transfer the data received from CPU No.2 to the devices set in the auto refresh parameter (CPU No.2 receive area) during END processing.

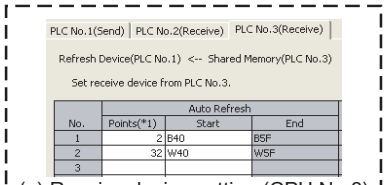


1) Data are written during END processing of CPU No.2.
2) Data are sent from CPU No.2 to CPU No.1 and No.3.
3) Data are read during END processing of CPU No.1.
4) Data are read during END processing of CPU No.3.

(d) Flow of data sent from CPU No.3 to other CPU modules

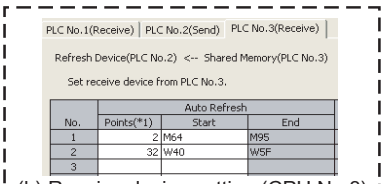
<Parameter setting>

Refer to those related to the data communications of CPU No.3 ((g) to (i)) among the auto refresh setting examples on Page 146, Section 6.1.2 (4) (a).



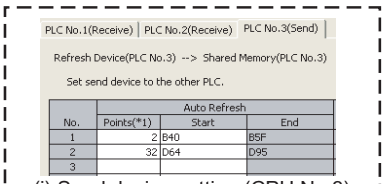
(g) Receive device setting (CPU No.3)

(1) Auto refresh setting of CPU No.1



(h) Receive device setting (CPU No.3)

(2) Auto refresh setting of CPU No.2

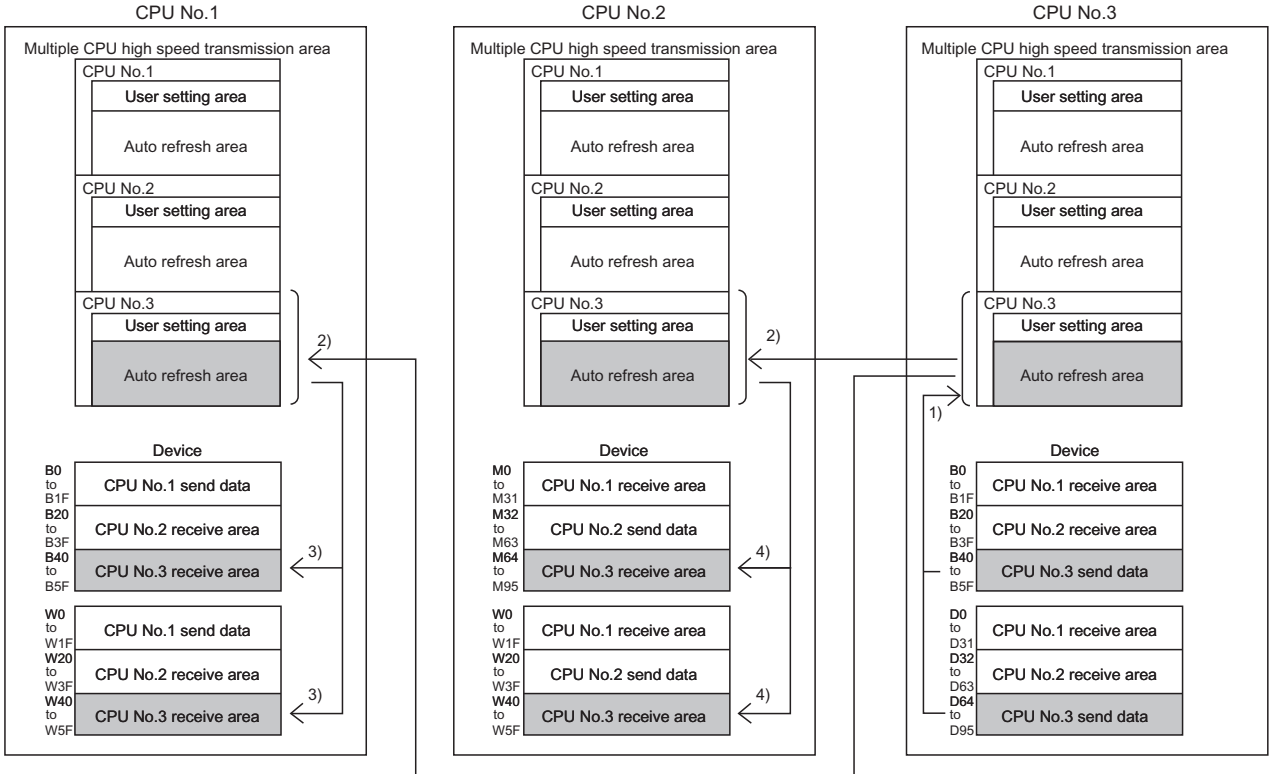


(i) Send device setting (CPU No.3)

(3) Auto refresh setting of CPU No.3

<Flow of data sent from CPU No.3 to other CPU modules>

- CPU No.3 writes data (CPU No.3 send data) in the devices set in the auto refresh parameter to its own auto refresh area during END processing.
- CPU No.3 sends the data stored in its own auto refresh area to CPU No.1 and No.2 in each multiple CPU high speed transmission cycle.
- CPU No.1 and No.2 transfer the data received from CPU No.3 to the devices set in the auto refresh parameter (CPU No.3 receive area) during END processing.



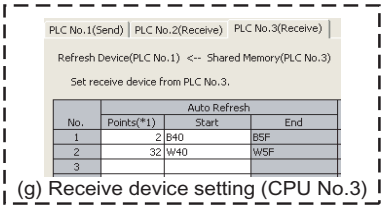
1) Data are written during END processing of CPU No.3.
2) Data are sent from CPU No.3 to CPU No.1 and No.2.
3) Data are read during END processing of CPU No.1.
4) Data are read during END processing of CPU No.2.

Point

If "Start" and "End" fields are left blank in "Auto Refresh Setting", auto refresh is not performed. (Only the receive area can be left blank.)

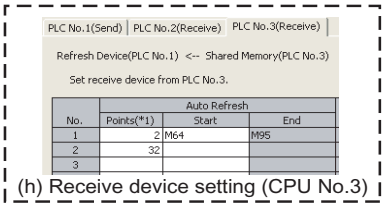
Ex. When the auto refresh setting of CPU No.2 is left blank in "Flow of data sent from CPU No.3 to other CPU modules" described on Page 149, Section 6.1.2 (4) (d)

CPU No.2 does not auto-refresh the data received from CPU No.3 to W40 to W5F.



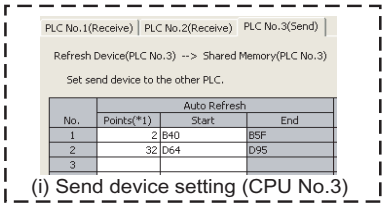
(g) Receive device setting (CPU No.3)

(1) Auto refresh setting of CPU No.1



(h) Receive device setting (CPU No.3)

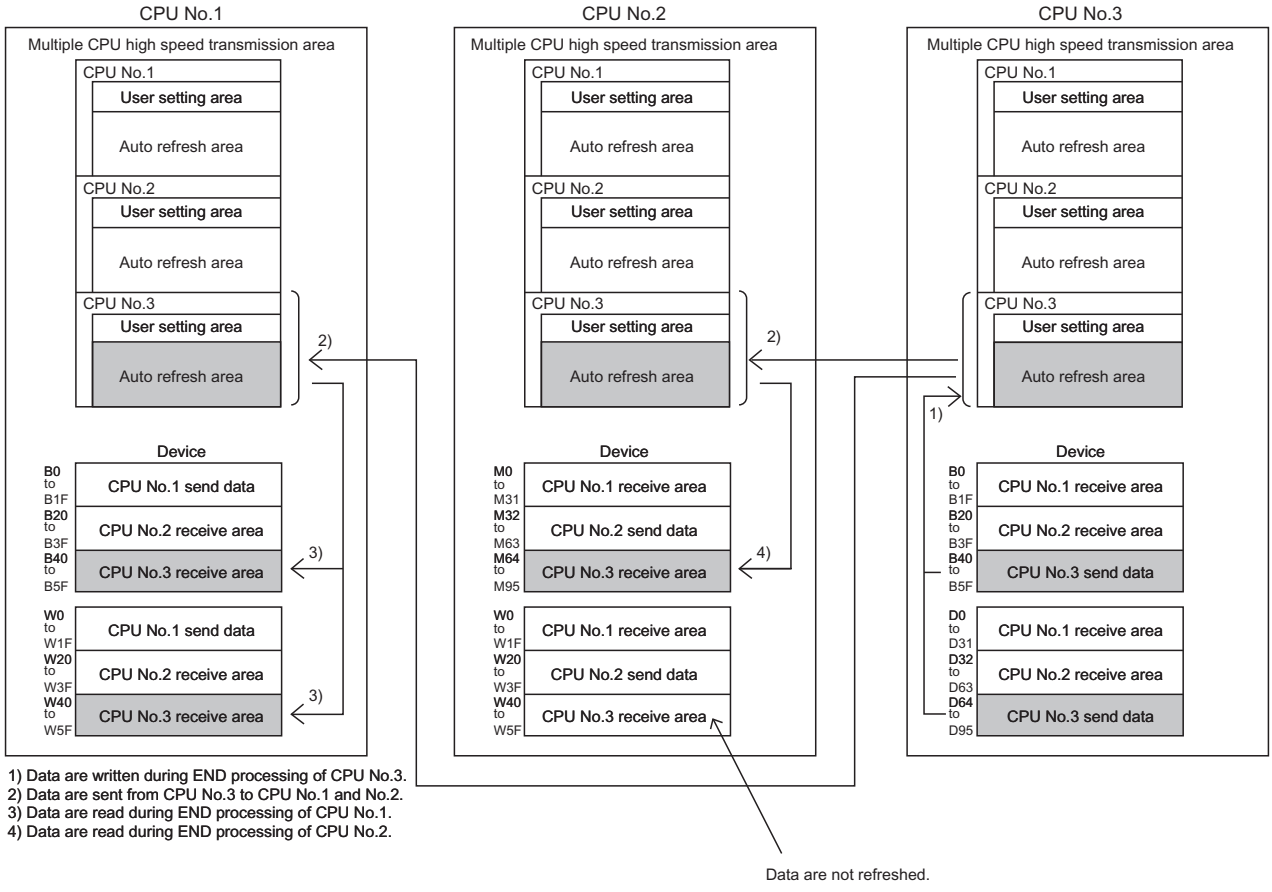
(2) Auto refresh setting of CPU No.2



(i) Send device setting (CPU No.3)

(3) Auto refresh setting of CPU No.3

For the flow of sending data from CPU No.3, refer to "Flow of sending data from CPU No.3 to other CPUs" on Page 149, Section 6.1.2 (4) (d).



(5) Precautions

(a) Local device setting

Device ranges set for the auto refresh target cannot be set as local devices. If set, the refresh data will not be updated.

(b) Using the same file name as that of the program in the file register

Do not set the file register of each program as an auto refresh target device. If set, data are automatically refreshed to the file register corresponding to the scan execution type program executed last.

(c) Transmission delay time

Data transmission delay time due to auto refresh is from 0.09ms to (1.80 + (sending side scan time + receiving side scan time × 2))ms.

(d) Assurance of send data

Old data and new data may coexist (data inconsistency) in each CPU module due to the timing of refreshing data in the host CPU module and reading data in other CPU modules.
The following are the methods to prevent data inconsistency in data communications by auto refresh.

- Preventing inconsistency of 32-bit data
  Data inconsistency will not occur because the data transmission by auto refresh is performed only in units of 32 bits (parameters are set in increments of 32 bits).

- Preventing inconsistency of data exceeding 32 bits
  With auto refresh, data are read in descending order of the setting number in auto refresh setting parameter. To prevent data inconsistency, use the setting number lower than the setting data as an interlock device.

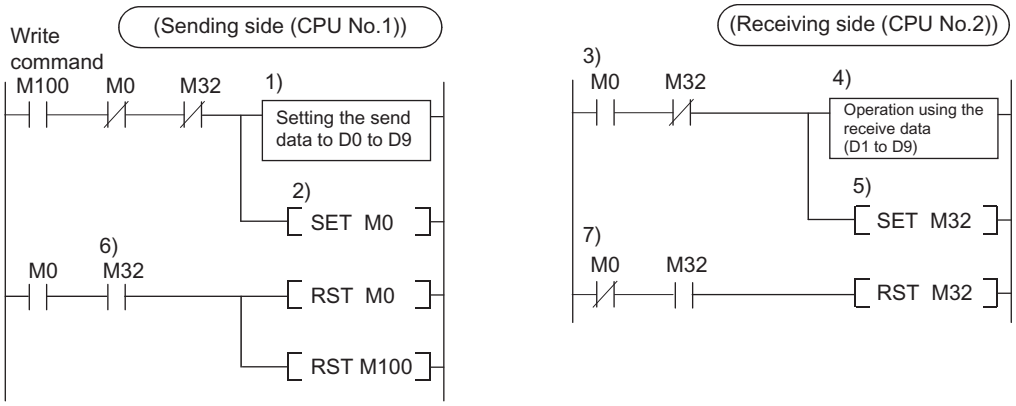
Ex. Program example for providing an interlock between CPU No.1 and No.2

[Parameter setting]

CPU No.1 auto refresh setting							Direction	CPU No.2 auto refresh setting						
PLC	Setting No.	CPU Specific Send Range			Auto Refresh			PLC	Setting No.	CPU Specific Send Range			Auto Refresh	
		Points	Start	End	Start	End				Points	Start	End	Start	End
PLC No.1	1	2	0	1	M0	M31	→	PLC No.1	1	2	0	1	M0	M31
	2	10	2	11	D0	D9			2	10	2	11	D0	D9
PLC No.2	1	2	0	1	M32	M63	←	PLC No.2	1	2	0	1	M32	M63

Use M0 as an interlock device of CPU No.1 (data setting complete bit) and M32 as an interlock device of CPU No.2 (receive data processing complete bit).

Program example (sending side) (CPU No.1)Program example (receiving side) (CPU No.2)]



1) CPU No.1 stores send data to D0 to D9.

2) CPU No.1 turns on the data setting complete bit (M0).

CPU No.1 transfers the data to the auto refresh area in its own CPU No.1 send area during END processing, and sends the transferred data to CPU No.2. CPU No.2 reads the received data from the auto refresh area in its own CPU No.1 send area and stores the data to the specified device during END processing.

3) CPU No.2 detects the send data set complete bit.

4) CPU No.2 performs the receive data processing.

5) CPU No.2 turns on the receive data processing complete bit (M32).

CPU No.2 writes the data of to the auto refresh area in its own CPU No.2 send area during END processing, and sends the written data to CPU No.1. CPU No.1 reads the received data from the auto refresh area in its own CPU No.2 send area and stores the data to the specified device during END processing.

6) CPU No.1 detects the on status of the receive data processing complete bit, and turns off the data set complete bit.

6.1.3 Communications by programs using the CPU shared memory

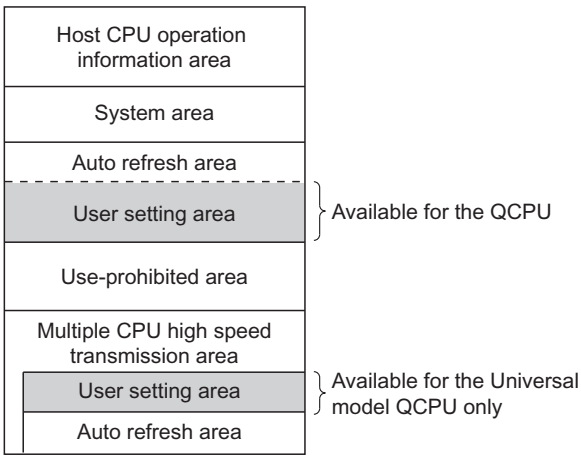
This section describes data communications by programs using the CPU shared memory.
The QCPU in the multiple CPU system communicates data by executing programs in the following cases.

- To read/write data from/to other CPU module (QCPU, C Controller module, or PC CPU module) in the system
- To read data in the CPU shared memory of the Motion CPU

(1) Areas used for data communications by programs

The following areas in the CPU shared memory are used.

- User setting area
- User setting area in the multiple CPU high speed transmission area



(a) Modules supporting data communications using the multiple CPU high speed transmission area

Only the following CPU modules can be used as communication-target modules of the Universal model QCPU using the user setting area in the multiple CPU high speed transmission area.

- Universal model QCPU (except the Q00UCPU, Q01UCPU, and Q02UCPU)
- Motion CPU (Q172DCPU(-S1), Q173DCPU(-S1), Q172DSCPU, or Q173DSCPU)
- C Controller module (Q12DCCPU-V, Q24DHCCPU-V, Q24DHCCPU-VG, Q24DHCCPU-LS, or Q26DHCCPU-LS)

(2) Instructions used to read/write data from/to the CPU shared memory

The QCPU in the multiple CPU system communicates data with other CPU modules by executing read/write instructions. The following read/write instructions can be used.

Item	Description
Write instruction*3*4	• Instructions using the cyclic transmission area device (U3En\G□)*1 • TO/DTO instructions (except for High Performance model QCPUs and Process CPUs) • S.TO instruction*2
Read instruction*3*4	• Instructions using the cyclic transmission area device (U3En\G□)*1 • FROM/DFRO instructions

*1 When accessing the multiple CPU high speed transmission area, the processing times of these instructions are shorter than those of the TO, DTO, FROM, and DFRO instructions.

*2 With this instruction, data cannot be written to the user setting area in the multiple CPU high speed transmission area.

*3 For details on the TO/DTO/S.TO instructions (for writing) and the FROM/DFRO instructions (for reading), refer to the following.

MELSEC-Q/L Programming Manual (Common Instruction)

*4 Motion CPUs do not support the use of these instructions.

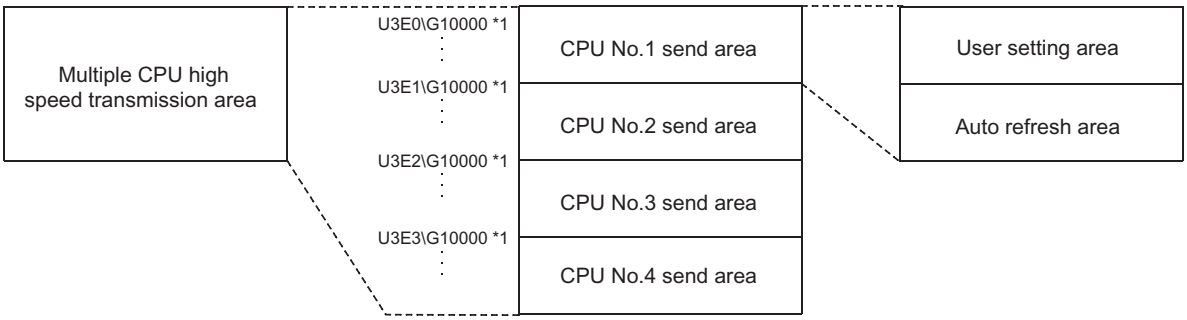
(3) Addresses of the user setting area and multiple CPU high speed transmission area

(a) Addresses of the user setting area

The addresses of the user setting area differ depending on the CPU module used. (☞Page 121, Section 6.1)

(b) Addresses of the multiple CPU high speed transmission area

The addresses of the multiple CPU high speed transmission area are shown below. The end addresses of the send areas in each CPU module differ depending on the number of points set in "CPU Specific Send Range" of PLC parameter ("Multiple CPU Setting").



*1 These addresses are used to specify the user setting area of the target CPU module in the cyclic transmission area device.

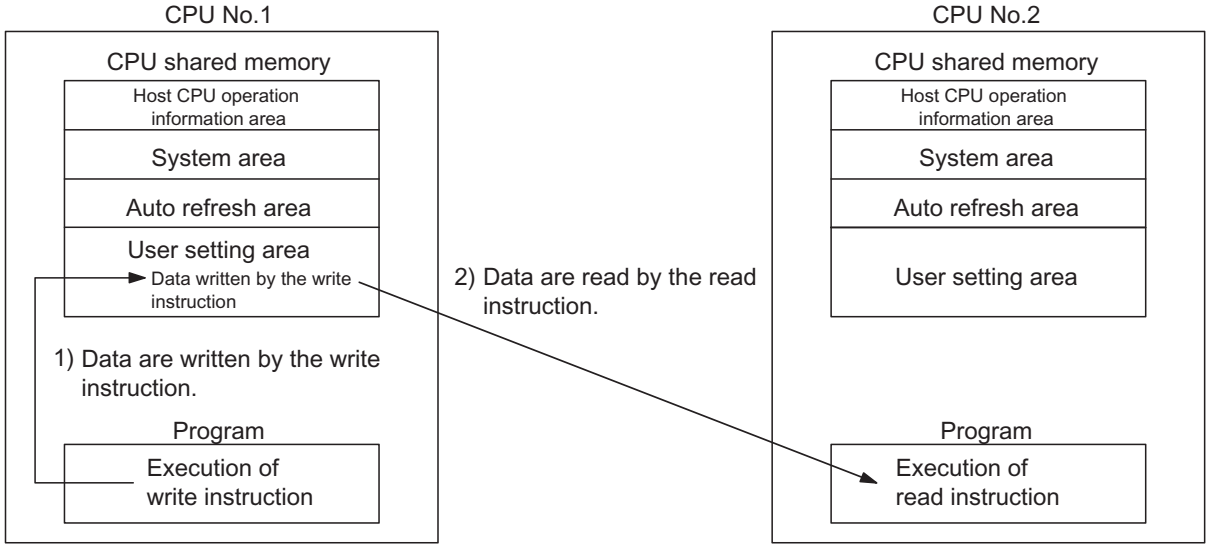
For details on each area in the multiple CPU high speed transmission area, refer to Page 138, Section 6.1.2.

(4) Overview (when the user setting area is used)

The data written to the CPU shared memory in the host CPU module by a write instruction can be read by other CPU modules by a read instruction.

Unlike the auto refresh using the CPU shared memory, the up-to-date data at the time of an instruction execution can be read directly.

The following shows the operations when data written to the CPU shared memory of CPU No.1 by a write instruction is read by CPU No.2 by a read instruction.



- Processing in CPU No.1

  1) CPU No.1 writes data to the user setting area of its own by the write instruction.

- Processing in CPU No.2

  2) CPU No.2 reads the data from the user setting area of CPU No.1 and stores the data in the specified device by the read instruction.

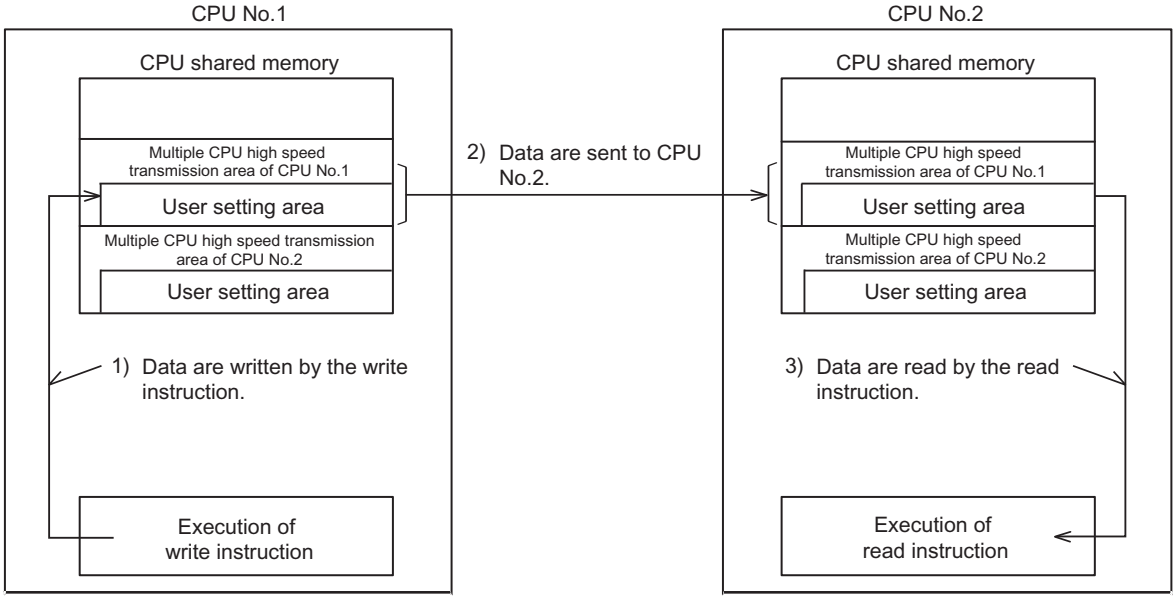
For the read/write instructions, refer to Page 154, Section 6.1.3 (2).

(5) Overview (when the user setting area in the multiple CPU high speed communication area is used)

The data written to the multiple CPU high speed transmission area of the host CPU module by a write instruction is sent to other CPU modules at regular intervals. Other CPU modules read the receive data by a read instruction.

Unlike the auto refresh using the CPU shared memory, the up-to-date data at the time of an instruction execution can be read directly.

The following shows the operation when data written to the CPU shared memory of CPU No.1 by a write instruction is read by CPU No.2 by a read instruction.



- Procedure for CPU No.2 to read device data of CPU No.1

  1) CPU No.1 writes data in the user setting area of the multiple CPU high speed transmission area of its own by the write instruction.

  2) CPU No.1 sends the stored data in the multiple CPU high speed transmission area to that of CPU No.2.

  3) CPU No.2 reads the received data and stores the data in the specified device by the read instruction.

For the write/read instructions, refer to Page 154, Section 6.1.3 (2).

Point

The delay time of data communications by programs using the user setting area in the multiple CPU high speed transmission area is from 0.09ms to 1.80ms.

(6) Parameter settings

To use the user setting area in the multiple CPU high speed transmission area, set the ranges (number of points) to be sent by each CPU module ("CPU Specific Send Range") in PLC parameter ("Multiple CPU Setting").
For setting details, refer to Page 138, Section 6.1.2.

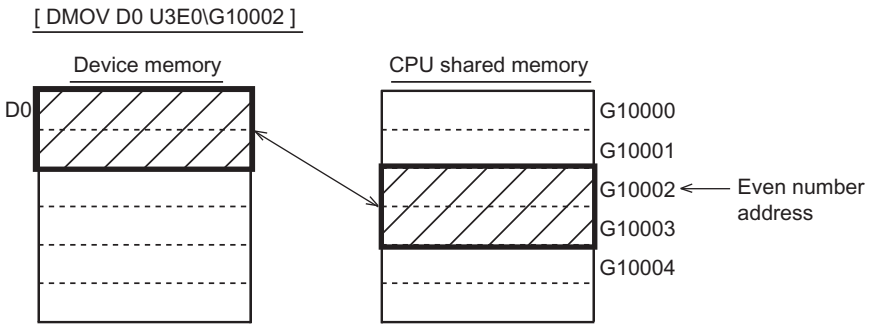
(7) Assurance of send data

Old data and new data may coexist (data inconsistency) in each CPU module due to the timing of reading data in the host CPU module and writing/sending data in other CPU modules. The following are the methods to prevent data inconsistency in data communications by programs using the CPU shared memory.

(a) Preventing inconsistency of 32-bit data

To prevent data inconsistency, access the user setting area in the CPU shared memory by specifying an even number as the start address.

Ex. Specifying "10002" as the start address



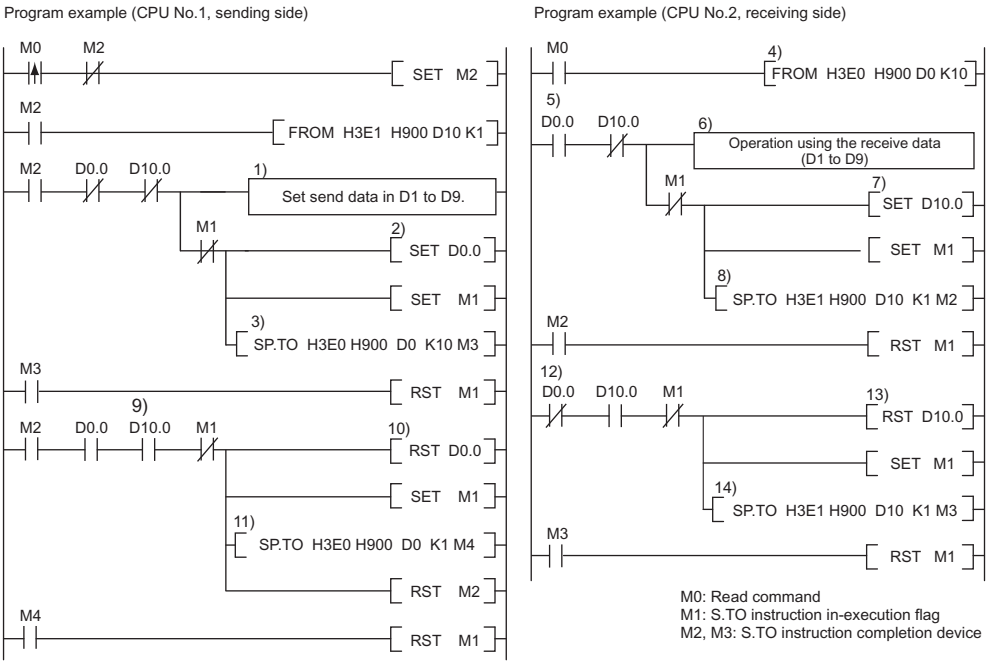
(b) Preventing inconsistency of data exceeding 32 bits

- When the user setting area is used

  The read instruction reads data in order starting from the start address to the end address of the user setting area. On the other hand, the write instruction writes data in order starting from the end address to the start address of the user setting area.

  To prevent data inconsistency, set an interlock device at the start of data to be communicated.

Ex. Program example for providing an interlock between CPU No.1 and No.2



1) CPU No.1 sets send data in D1 to D9.
2) CPU No.1 turns on the send data setting complete flag (D0.0).
3) CPU No.1 writes the send data (D1 to D9) to the user setting area of its own.

4) CPU No.2 reads the send data from the user setting area of CPU No.1.
5) CPU No.2 detects the on status of the send data setting complete flag (D0.0).
6) CPU No.2 reads the receive data from D1 to D9.
7) CPU No.2 turns on the receive data processing complete flag (D10.0).
8) CPU No.2 writes the status of the receive data processing complete flag to the user setting area of CPU No.2.

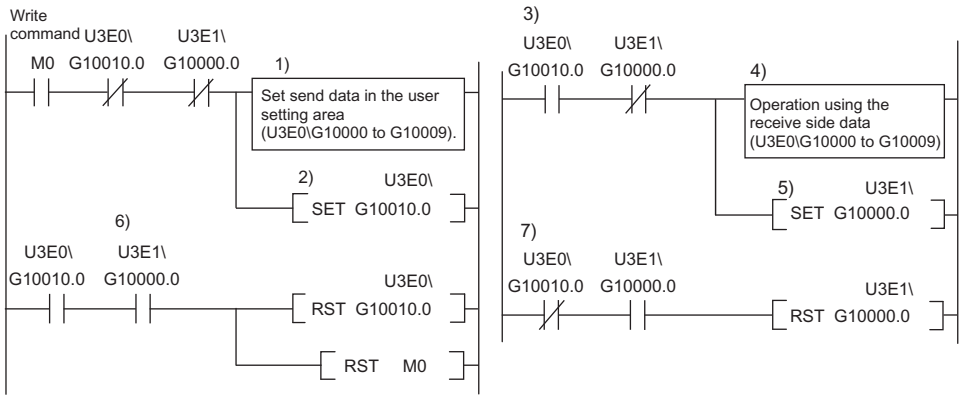
9) CPU No.1 detects the on status of the receive data processing complete flag (D10.0.
10) CPU No.1 turns off the send data setting complete flag (D0.0).
11) CPU No.1 writes the status of the send data setting complete flag to the user setting area of CPU No.1.

12) CPU No.2 detects the off status of the send data setting complete flag (D0.0).
13) CPU No.2 turns off the receive data processing complete flag (D10.0).
14) CPU No.2 writes the status of the receive data processing complete flag to the user setting area of CPU No.2.

- When the user setting area in the multiple CPU high speed transmission area is used
  The read instruction reads data in order of those were written to the user setting area. To prevent data inconsistency, use the device written after the transfer data as an interlock regardless of the device type and address.

Ex. Program example for providing an interlock between CPU No.1 and No.2

Program example (CPU No.1, sending side) Program example (CPU No.2, receiving side)



1) CPU No.1 writes send data to the user setting area.
2) CPU No.1 writes the on status of the send data setting complete bit to the user setting area.

<Sending data in the multiple CPU high speed transmission area of CPU No.1 to CPU No.2>
3) CPU No.2 detects the on status of the send data setting complete bit.
4) CPU No.2 performs receive data processing.
5) CPU No.2 writes the on status of the receive data processing complete bit to the user setting area.

<Sending data in the multiple CPU high speed transmission area of CPU No.2 to CPU No.1>
6) CPU No.1 detects the on status of the receive data processing complete it, and turns off the send data setting complete bit.

<Sending data in the multiple CPU high speed transmission area of CPU No.1 to CPU No.2>
7) CPU No.2 detects the on status of the send data setting complete bit, and turns off the receive data processing complete bit.

Remark

With an instruction such as the BMOV instruction, which writes two-word or more data to the user setting area, data are written in order from the end address to the start address.
When writing the send data and interlock signal together with one instruction, provide an interlock signal at the start of send data to prevent data inconsistency.

(8) Precautions

(a) Start I/O numbers of CPU modules

Set the following start I/O numbers to each CPU module for the read/write instructions.

CPU No.	CPU No.1	CPU No.2	CPU No.3	CPU No.4
Start I/O number	$3E0_H$	$3E1_H$	$3E2_H$	$3E3_H$

(b) Writing data to the CPU shared memory

Do not write data to the following areas in the CPU shared memory. (☞ Page 121, Section 6.1)

- System area
- Auto refresh area
- Use-prohibited area

(c) Reading data from the CPU shared memory

Do not read data from the following areas in the CPU shared memory when a High Performance model QCPU or Process CPU is used.(☞ Page 121, Section 6.1)

- System area
- Auto refresh area

(d) Accessing a module in RESET status

No error will occur even if the CPU module accessed by a read instruction is in RESET status.
However, the SM390 (access execution flag) will remain off even after the instruction execution has been completed. (This will not apply to Universal model QCPUs.)

(e) Accessing CPU modules simultaneously

Configure an interlock to prevent simultaneous access during data communications by the read/write instructions. If accessed, old data and new data may coexist (data inconsistency). (☞ Page 157, Section 6.1.3 (7))

(f) Writing data to the CPU shared memory of other CPU modules

Data cannot be written to the CPU shared memory of other CPU modules by a write instruction.
If data are written by executing the TO, S.TO instructions or those using the cyclic transmission area device (U3En\G□), "SP. UNIT ERROR" (error code: 2115) will occur.

(g) Writing data to the CPU shared memory of its own

- Basic model QCPU
  Data can be written with any write instruction.

- High Performance model QCPU or Process CPU
  Data can be written with the S.TO instruction.
  However, data cannot be written with instructions using the cyclic transmission area device (U3En\G□). If used, "SP.UNIT ERROR" (error code: 2114) will occur.

- Universal model QCPU
  Data can be written with any write instruction.

(h) Reading data from the CPU shared memory

- Basic model QCPU
  Data can be read with any read instruction.

- High Performance model QCPU or Process CPU
  Data cannot be read with any read instruction.
  If read, "SP.UNIT ERROR" (error code: 2114) will occur.

- Universal model QCPU
  Data can be read with any read instruction.

(i) Accessing a CPU module that is not actually mounted

A CPU module that is not actually mounted cannot be accessed with instructions using the cyclic transmission area device(U3En\G□). If accessed, "SP.UNIT ERROR" (error code: 2110) will occur.

6.1.4 Communications among CPU modules when an error is detected

This section describes the operations performed when an error is detected during data communications among CPU modules using the CPU shared memory.

(1) Operation when improper data is received

If a CPU module receives improper data during data communications among CPU modules due to noise or failure, the module discards the receive data. If the receive data is discarded, the CPU module holds the data which was received before the discarded data.
When the module receives proper data next, the data will be updated.

(2) Data transmission when an error is detected

The operation status of auto refresh and data communications among CPU modules when the host CPU module has detected a self-diagnostics error will be as follows.

○: Transferred ×: Not transferred

Error definition		Auto refresh*1	Data communications among CPU modules*2
Minor error		○	○
Moderate error	Factors other than below	○	○
	Multiple CPU high-speed transmission function parameter error (including the consistency check error)	×*4	×*3*4
Major error		×	×*3

*1 Auto refresh means data transfer between the internal user devices and the multiple CPU high-speed transmission area in the host CPU module.

*2 Data communications among CPU modules means data communications between the multiple CPU high-speed transmission area in the host CPU module and the multiple CPU high-speed transmission area in other CPU modules.

*3 If an error occurs during the normal operation, transmission of the normal data before the error is continued.
Even if data are written to the multiple CPU high-speed transmission area after the error, the data will not be sent to other CPU modules.

*4 If a consistency check error occurs due to PLC parameter change during the normal operation, both auto refresh and data communications among CPU modules are continued.

(3) Applicable CPU modules

The above operations are performed when any of the following CPU modules is used.

- Universal model QCPU (except the Q00UCPU, Q01UCPU, and Q02UCPU)
- Motion CPU (Q172DCPU(-S1), Q173DCPU(-S1), Q172DSCPU, or Q173DSCPU)
- C Controller module (Q12DCCPU-V, Q24DHCCPU-V, Q24DHCCPU-VG, Q24DHCCPU-LS, or Q26DHCCPU-LS)

6.2 Control Directions from QCPU to Motion CPU

Control directions can be issued from the QCPU to Motion CPU in a multiple CPU system by using the following motion dedicated instructions. (Control directions cannot be issued from the Motion CPU to another Motion CPU.)
For details on the motion dedicated instructions and their availabilities, refer to the manual for the motion CPU used.

○: Available, ×: Not available

Instruction	Description	QCPU		
		Basic model QCPU, High Performance model QCPU, Process CPU	Q00UCPU, Q01UCPU, Q02UCPU	Universal model QCPU (except the Q00UCPU, Q01UCPU, and Q02UCPU)
S.SFCS, SP.SFCS	Requests startup of the motion SFC program.	○	○	×
D.SFCS, DP.SFCS		×	×	○
S.SVST*1, SP.SVST*1	Requests the start of the servo program.	○	○	×
D.SVST, DP.SVST		×	×	○
S.CHGV*1, SP.CHGV*1	Changes the speed of the axes during positioning and JOG operations.	○	○	×
D.CHGV, DP.CHGV		×	×	○
D.CHGVS*3, DP.CHGVS*3	Changes the speed of the command generation axes during positioning and JOG operations.	×	×	○
S.CHGT*1, SP.CHGT*1	Changes the torque control value during operation and suspension when in real mode.	○	○	×
D.CHGT, DP.CHGT		×	×	○
D.CHGT2*2, DP.CHGT2*2	Individually changes the torque control value during operation and suspension.	×	×	○
S.CHGA*1, SP.CHGA*1	Changes the current values of the halted axes, the synchronized encoder, and the cam axes.	○	○	×
D.CHGA, DP.CHGA		×	×	○
D.CHGAS*3, DP.CHGAS*3	Changes the current values of halted command generation axes.	×	×	○

*1 To execute these instructions, the following restrictions on the version of the Motion CPU apply.
- Q172CPUN(-T), Q173CPUN(-T), Q172HCPU(-T), and Q173HCPU(-T): There is no restriction.
- Q172CPU: Version N or later
- Q173CPU: Version M or later

*2 To execute these instructions, use any of the following Motion CPUs.
- Q172DSCPU
- Q173DSCPU

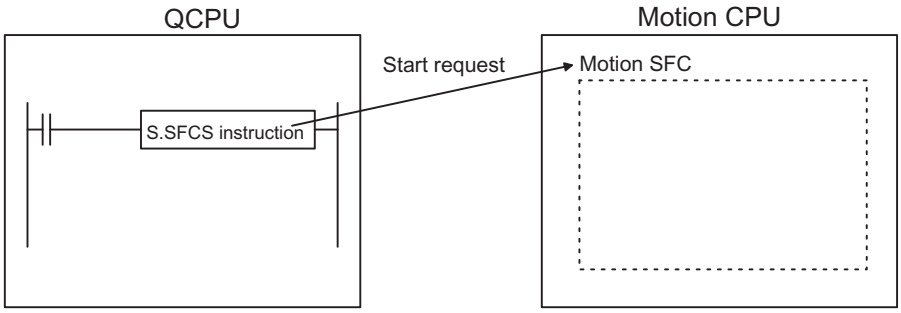
*3 To execute these instructions, use any of the following Motion CPUs.
- Q172DSCPU (when version 00B or later of operating system software SW8DNC-SV22QL is used)
- Q173DSCPU (when version 00B or later of operating system software SW8DNC-SV22QJ is used)

Remark

C Controller modules have functions that direct control to Motion CPUs. (Manual for the C Controller module used)

Ex. S.SFCS instruction

The motion SFC programs in a Motion CPU can be started up from the QCPU.



Point

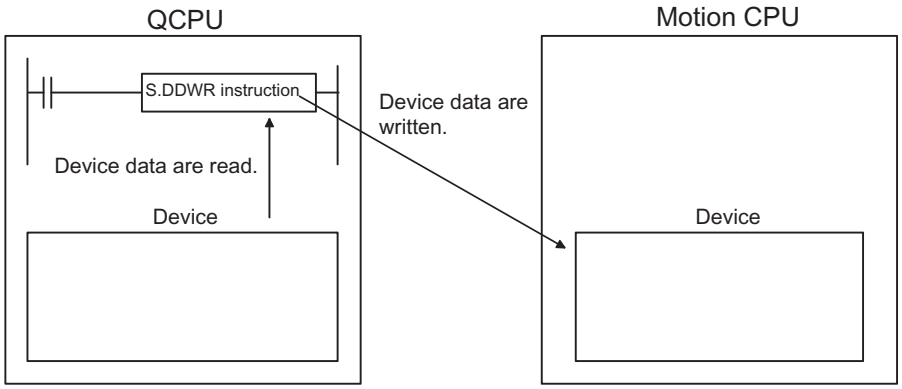
One QCPU can execute up to total of 32 motion dedicated instructions and multiple CPU transmission dedicated instructions (except the S(P).GINT instruction) simultaneously.
Note that if a motion dedicated instruction and a multiple CPU transmission dedicated instruction are executed simultaneously, processing of the instruction received first is performed first. If 33 or more unprocessed instructions are accumulated, "OPERATION ERROR" (error code: 4107) will occur.

6.3 Communications Among CPU Modules By Dedicated Instructions

6.3.1 Reading/writing device data from/to Motion CPU

The QCPU can read/write device data from/to the Motion CPU by executing the multiple CPU transmission dedicated instructions and multiple CPU high-speed transmission dedicated instructions. (The Motion CPU cannot read/write device data from/to other CPU modules including the Motion CPU.)
For details on these two instructions and their availabilities, refer to the manual for the Motion CPU used.

Ex. S.DDWR instruction
The device data in the QCPU are written to the devices in the Motion CPU.



(1) Multiple CPU transmission dedicated instructions

The QCPU reads/writes device data from/to the Q172CPUN(-T), Q173CPUN(-T), Q172HCPU(-T), and Q173HCPU(-T) by executing the multiple CPU transmission dedicated instructions listed below.

○: Available, ×: Not available

Instruction	Description	QCPU		
		Basic model QCPU, High Performance model QCPU, Process CPU	Q00UCPU, Q01UCPU, Q02UCPU	Universal model QCPU (except the Q00UCPU, Q01UCPU, and Q02UCPU)
S.DDWR, SP.DDWR	Writes device data in the host CPU module to the devices in other CPU modules.	○	○	×
S.DDRD, SP.DDRD	Loads device data in other CPU modules to the devices in the host CPU module.	○	○	×
S.GINT, SP.GINT	Requests startup of interrupt programs in other CPU modules.	○	○	×

(2) Multiple CPU high-speed transmission dedicated instructions

The Universal model QCPU reads/writes device data from/to the Q172DCPU(-S1), Q173DCPU(-S1), Q172DSCPU, and Q173DSCPU by executing the multiple CPU high-speed transmission dedicated instructions listed below.

○: Available, ×: Not available

Instruction	Description	QCPU	
		Q00UCPU, Q01UCPU, Q02UCPU	Universal model QCPU (except the Q00UCPU, Q01UCPU, and Q02UCPU)
D.DDWR, DP.DDWR	Writes device data in the host CPU module to the devices in other CPU modules.	×	○
D.DDRD, DP.DDRD	Loads device data in other CPU modules to the devices in the host CPU module.	×	○
D.GINT, DP.GINT	Requests startup of interrupt programs in other CPU modules.	×	○

Point

One QCPU can execute up to total of 32 motion dedicated instructions and multiple CPU transmission dedicated instructions (except the S(P).GINT instruction) simultaneously.
Note that if a motion dedicated instruction and a multiple CPU transmission dedicated instruction are executed simultaneously, processing of the instruction received first is performed first. If 33 or more unprocessed instructions are accumulated, "OPERATION ERROR" (error code: 4107) will occur.

Remark

C Controller modules have functions that direct control to Motion CPUs. (Manual for the C Controller module used)

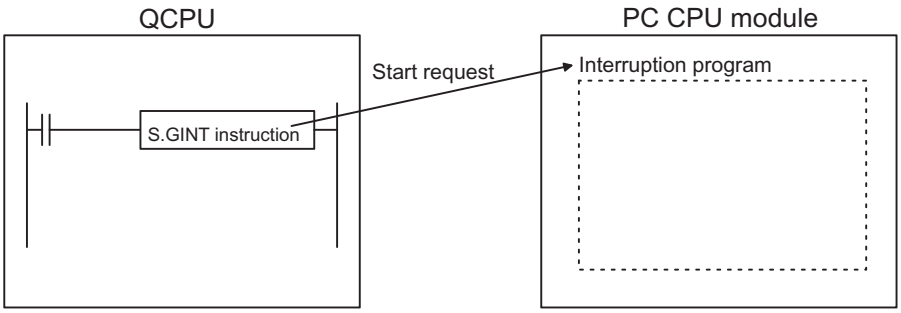
6.3.2 Starting interrupt programs

The QCPU can start interrupt programs to the C controller unit/PC CPU module by executing the multiple CPU transmission dedicated instructions and multiple CPU high-speed transmission dedicated instructions.

Instruction	Description
S.GINT, SP.GINT	Requests startup of interrupt programs in other CPU modules. For the availabilities, refer to the following. Manual for the C Controller module used Manual for the PC CPU module used
D.GINT, DP.GINT	

Interrupt programs can be started from a C Controller module to a Motion CPU or another C Controller module.
(Manual for the C Controller module used)
Interrupt programs cannot be started from a PC CPU module.

Ex. S.GINT instruction
Interrupt programs can be started from the QCPU to the PC CPU module.



6.3.3 Reading/writing device data between QnUCPUs

The Universal model QCPU can read/write device data from/to another Universal model QCPU by executing the multiple CPU high-speed transmission dedicated instructions listed below.

○: Available, ×: Not available

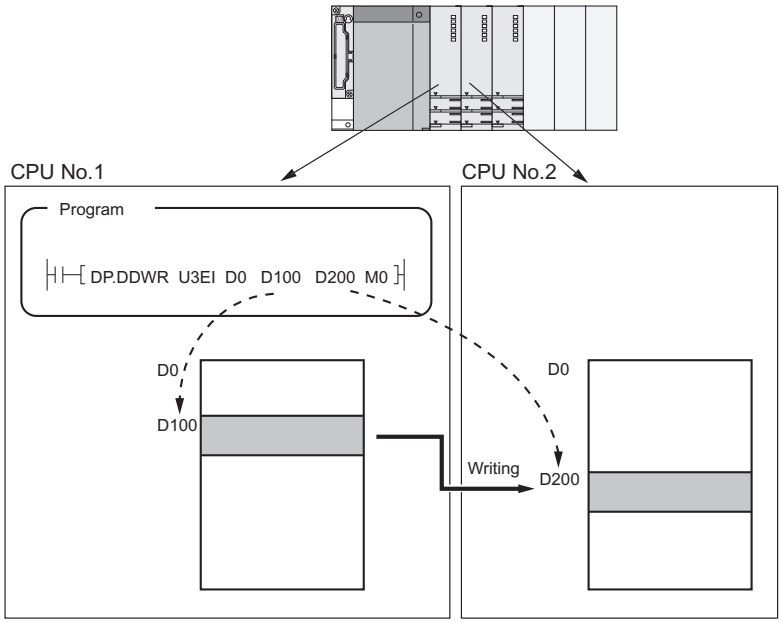
Instruction*2	Description	QCPU		
		Basic model QCPU, High Performance model QCPU, Process CPU	Q00UCPU, Q01UCPU, Q02UCPU	Universal model QCPU (except the Q00UCPU, Q01UCPU, and Q02UCPU)*1
D.DDRD, DP.DDRD	Loads device data in other CPU modules to the devices in the host CPU module.	×	×	○
D.DDWR, DP.DDWR	Writes device data in the host CPU module to the devices in other CPU modules.	×	×	○

*1 For the Q03UDCPU, Q04UDHCPU, and Q06UDHCPU, the module with a serial number (first five digits) of "10012" or later must be used.

*2 For details on the multiple CPU high-speed transmission dedicated instructions, refer to the following.

MELSEC-Q/L Programming Manual (Common Instruction)

The following is the operation to write device data in CPU No.1 to the device of CPU No.2 by executing the DP.DDWR instruction.



6.4 Multiple CPU Synchronous Interrupt

This function executes interrupt programs (multiple CPU synchronous interrupt programs) at the start timing of each multiple CPU high speed transmission cycle. The function enables data communications among CPU modules in synchronization with the multiple CPU high speed transmission cycles.
Since the multiple CPU high speed transmission cycles are synchronized with the Motion CPU operation cycles, use of the function enables faster responses to the requests from a Motion CPU and sequence program execution synchronized with the Motion CPU operation cycles.

(1) Multiple CPU synchronous interrupt programs

Multiple CPU synchronous interrupt program is a program using an interrupt pointer (I45). A sequence of instructions from an interrupt pointer (I45) to the IRET instruction is a multiple CPU synchronous interrupt program.

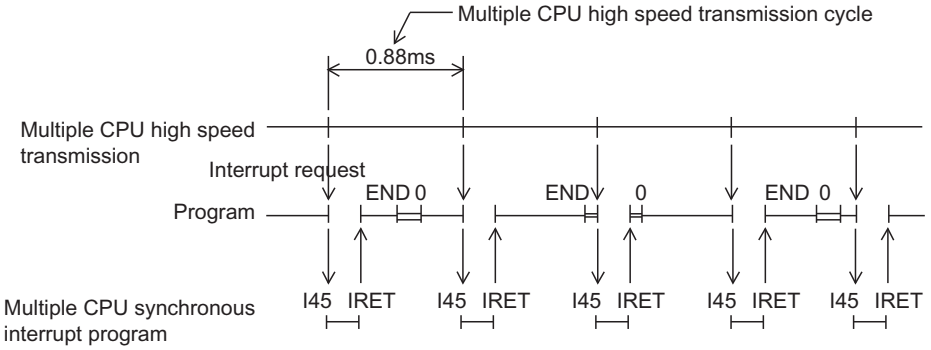
To execute multiple CPU synchronous interrupt programs, enable the execution of interrupt programs using the EI instruction.*1*2

*1 The setting is not required on the Motion CPU side.

*2 Register the routine corresponding to the multiple CPU synchronous interrupt using the bus interface function of the C Controller module. (Manual for the C Controller module used)

(2) Execution timing

Multiple CPU synchronous interrupt programs are executed at the start timing of each multiple CPU high speed transmission cycle.

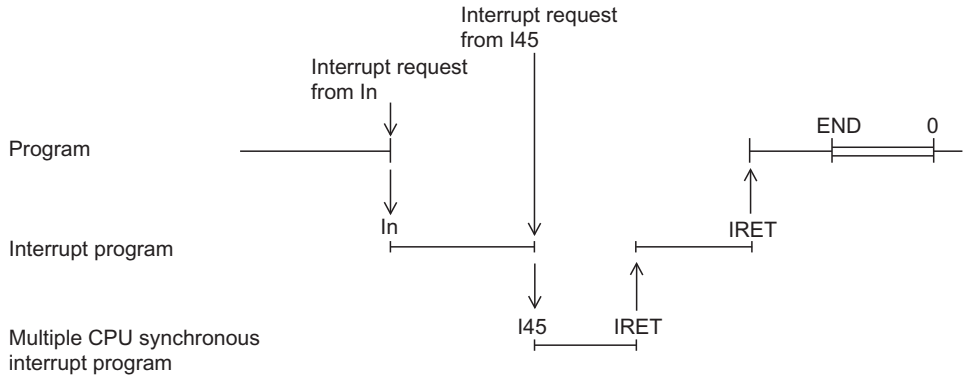


(3) Applicable CPU modules

The multiple CPU synchronous interrupt function can be executed when any of the following CPU modules is used.

- Universal model QCPU (except the Q00UCPU, Q01UCPU, and Q02UCPU)
- Motion CPU (Q172DCPU(-S1), Q173DCPU(-S1), Q172DSCPU, or Q173DSCPU)
- C Controller module (Q12DCCPU-V, Q24DHCCPU-V, Q24DHCCPU-VG, Q24DHCCPU-LS, and Q26DHCCPU-LS)

If a multiple CPU synchronous interrupt is requested during the execution of another interrupt program, the CPU module stops the running program and execute the multiple CPU synchronous interrupt program.



(4) Operation when an interrupt factor occurs and restrictions on programming

For the operation when an interrupt factor occurs and the restrictions on programming, refer to the following.

User's Manual (Function Explanation, Program Fundamentals) for the CPU module used

6.5 Multiple CPU synchronous startup

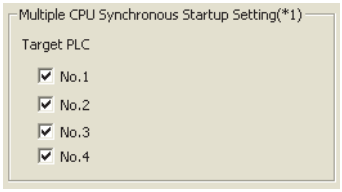
This function synchronizes the startups of CPU No.1 to No.4.
Since the function monitors the startup of each CPU module, an interlock program normally used to check the startup of another CPU module before accessing is no longer required. This function, however, synchronizes the startups with the slowest one. As a result, the startup of the system may be slow.

Point

This is the function to access each CPU module in a multiple CPU system without an interlock, not to start operations simultaneously among CPU modules after startup.

(1) Parameter setting

To use the function, select target CPU modules in "Multiple CPU Synchronous Startup Setting" of PLC parameter ("Multiple CPU Setting") using the programming tool. All the CPU modules are selected by default. (The startups of all the CPU modules are synchronized.)



Setting of this parameter must be the same for all the CPU modules in the system.
If not, "PARAMETER ERROR" (error code: 3015) will be detected.

(2) Applicable CPU modules

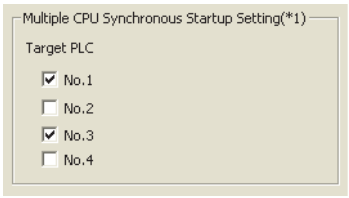
The multiple CPU synchronous startup function can be executed when any of the following CPU modules is used.

- Universal model QCPU (except the Q00UCPU, Q01UCPU, and Q02UCPU)
- Motion CPU (Q172DCPU(-S1), Q173DCPU(-S1), Q172DSCPU, or Q173DSCPU)
- C Controller module (Q12DCCPU-V, Q24DHCCPU-V, Q24DHCCPU-VG, Q24DHCCPU-LS, or Q26DHCCPU-LS)

(3) Precautions

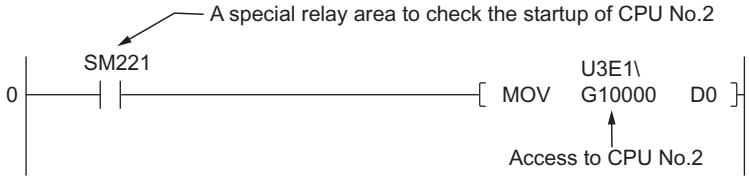
If a CPU module that does not support this function is used, uncheck the checkbox of the corresponding CPU number in PLC parameter.

Ex. When High Performance model QCPUs are used as CPU No.2 and No.4
Uncheck the checkboxes of CPU No.2 and No.4.



Remark

If this function is not used (each CPU module starts up asynchronously), create a program to check the startup of each CPU module using SM220 (CPU No.1 preparation completed) to SM223 (CPU No.4 preparation completed).



APPENDICES

Appendix 1 Parameters for a Multiple CPU System

(1) Parameters required

For a multiple CPU system, the following PLC parameters shall be set additionally to those for a single CPU system.

- "Multiple CPU Setting"
- "Control PLC" setting in "Detailed Setting" of "I/O Assignment"

The same PLC parameters must be set to all the CPU modules used in a multiple CPU system, except some parameters. (☞Page 175, Appendix 1.1)

When a PC CPU module is used, the multiple CPU parameters set in the programming tool can be used as is in PC CPU setting utility.

(2) When parameters for the multiple CPU system have been changed

Set the same parameters to all the CPU modules in the system, and reset CPU No.1 or power off and on the system.

The multiple CPU parameters set for a project can be used as is for another project. (☞Page 88, Section 4.2.2 (2))

(3) Checking the multiple

In a multiple CPU system, whether the same multiple CPU parameters are set to all the CPU modules is checked at the following timing.

- When a multiple CPU system is powered on
- When CPU No.1 is reset
- When the operating status of the CPU modules are switched from STOP to RUN
- When any parameter is changed

This check is called a consistency check. (For the parameters to be checked, refer to the items marked ○ and △ in the Consistency column on Page 175, Appendix 1.1. For check details, refer to Page 174, Appendix 1 (3) (b).)

(a) When same parameters are set to all the CPU modules

The multiple CPU system starts up.

(b) When same parameters are not set to all the CPU modules

The multiple CPU system performs either of the operations described in the following table.

Check the multiple CPU parameters, and set the same parameters to all the CPU modules in the system. To start the system, reset CPU No.1 or power off and on the system. (☞Page 105, Section 4.6)

<table>
<tr><th colspan="2">Item</th><th>CPU No.1</th><th>Other than CPU No.1</th></tr>
<tr><td colspan="2">The multiple CPU system is powered on.</td><td rowspan="2">No consistency check of the multiple CPU parameters is performed.*1</td><td rowspan="2">• The CPU module compares its parameters with those of CPU No.1.
• "PARAMETER ERROR" (error code: 3012/3015) will occur in the CPU module if the parameters do not match with those of CPU No.1.</td></tr>
<tr><td colspan="2">CPU No.1 is reset.</td></tr>
<tr><td rowspan="3">• The RUN/STOP switch is switched from STOP to RUN.
• Parameters are written from a programming tool.</td><td>The operating status of any CPU module is in RUN.</td><td colspan="2">• The CPU module compares its parameters with those of a running CPU module with the lowest No.*2
• "PARAMETER ERROR" (error code: 3012/3015) will occur in the CPU module if the parameters do not match.</td></tr>
<tr><td>There is no CPU module whose operating status is in RUN.</td><td>• The CPU module compares its parameters with those of CPU No.2 (in the STOP status).*2
• "PARAMETER ERROR" (error code: 3012/3015) will occur in the CPU module if the parameters do not match with those of CPU No.2.</td><td>• The CPU module compares its parameters with those of CPU No.1.
• "PARAMETER ERROR" (error code: 3012/3015) will occur in the CPU module if the parameters do not match with those of CPU No.1.</td></tr>
<tr><td>A stop error has occurred in CPU No.1.</td><td>-</td><td>Since "MULTI CPU DOWN" (error code: 7000) error occurs in the CPU module, the module will not start running. (No consistency check is performed.)</td></tr>
</table>

*1 Universal model QCPUs perform consistency check. "PARAMETER ERROR" (error code: 3015) will occur in the CPU module if the parameters do not match.

*2 Universal model QCPUs compare its parameters with those of CPU No.1.

Point

In a multiple CPU system containing a Motion CPU, if multiple CPU parameters not available for Motion CPUs are changed for a QCPU or PC CPU module, reset the QCPU used as CPU No.1 or power off and on the programmable controller system.

A High Performance model QCPU, Process CPU, or PC CPU module performs consistency check with the multiple CPU parameters of the Motion CPU, and detects "PARAMETER ERROR" (error code: 3015).

Appendix 1.1 List of parameters

(1) For Basic model QCPU, High Performance model QCPU, and Process CPU

The following table lists PLC parameters need to be set for a Basic model QCPU, High Performance QCPU, or Process CPU.

PLC parameter			Setting[*1]	Consistency[*2]	Reference
I/O Assignment	I/O Assignment	Type	-	○	Qn(H)/QnPH/QnPRH User's Manual (Function Explanation, Program Fundamentals)
		Model Name	-	-	
		Points	-	○	
		Start XY	-	○	
	Base Setting	Base Model Name	-	-	
		Power Model Name	-	-	
		Extension Cable	-	-	
		Slots	-	○	
	Switch Settings		-	-	
	Detailed Settings	Error Time Output Mode	-	-	
		PLC Operation Mode at H/W Error	-	-	
		I/O Response Time	-	-	
		Control PLC	○	○	Page 83, Section 4.2.2
PLC System	Points Occupied by Empty Slot		-	○	Qn(H)/QnPH/QnPRH User's Manual (Function Explanation, Program Fundamentals)
Multiple CPU Setting	No. of PLC		○	○	Page 83, Section 4.2.2
	Operation Mode		△	○	
	Online Module Change[*3]		○	△	
	All CPUs Can Read All Inputs		△	△	
	All CPUs Can Read All Outputs		△	△	
	Communication Area Setting (Refresh Setting)	CPU Specific Send Range	△	○	
		PLC Side Device	△	-	

*1
- ○ : Item that must be set in a multiple CPU system (A system does not operate without setting.)
- △ : Item that is set if needed in a multiple CPU system
- - : Item that is the same as in a single CPU system

*2
- ○ : Item that must have same settings among all the CPU modules in a multiple CPU system
- △ : Item that must have same settings among all the QCPUs and PC CPU module in a multiple CPU system (item that is not supported in Motion CPUs)
- - : Item that can be set individually for each CPU module in a multiple CPU system

*3 For a Basic model QCPU, the online module change setting is disabled.
High Performance model QCPUs do not support the online change function. To replace a module controlled by a Process CPU online, check the "Enable Online Module Change with Another PLC." checkbox.

(2) For Universal model QCPU

The following table lists PLC parameters need to be set for a Universal model QCPU.

PLC parameter				Setting[*1]	Consistency[*2]	Reference
I/O Assignment	I/O Assignment	Type		-	○	QnUCPU User's Manual (Function Explanation, Program Fundamentals)
		Model Name		-	-	
		Points		-	○	
		Start XY		-	○	
	Base Setting	Base Model Name		-	-	
		Power Model Name		-	-	
		Extension Cable		-	-	
		Slots		-	○	
	Switch Settings			-	-	
	Detailed Settings	Error Time Output Mode		-	-	
		PLC Operation Mode at H/W Error		-	-	
		I/O Response Time		-	-	
		Control PLC		○	○	Page 83, Section 4.2.2
PLC System	Points Occupied by Empty Slot			-	○	QnUCPU User's Manual (Function Explanation, Program Fundamentals)
Multiple CPU Setting	No. of PLC			○	○	Page 83, Section 4.2.2
	Host Station			△	-	Page 26, Section 2.1, Page 83, Section 4.2.2
	Operation Mode			△	○	Page 83, Section 4.2.2
	Multiple CPU Synchronous Startup Setting[*4]			△	○	
	Online Module Change[*4]			△	○	
	All CPUs Can Read All Inputs			△	△	
	All CPUs Can Read All Outputs			△	△	
	Multiple CPU high Speed Transmission Area Setting[*4]	Use Multiple CPU High Speed Transmission		○	○	
		CPU Specific Send Range		○	○	
		Auto Refresh	Points	△	△	
			Start	△	-	
		Advanced Settings		△	○	
		System Area[*3]		△	-	
	Communication Area Setting (Refresh setting)	CPU Specific Send Range		△	○/△[*5]	
		PLC Side Devices		△	-	

*1
○ : Item that must be set in a multiple CPU system (A system does not operate without setting.)
△ : Item that is set if needed in a multiple CPU system
- : Item that is the same as in a single CPU system

*2
○ : Item that must have same settings among all the CPU modules in a multiple CPU system
△ : Item that must have same settings among all the QCPUs and PC CPU module in a multiple CPU system (item that is not supported in Motion CPUs)
- : Items that can be set individually for each CPU module in a multiple CPU system

*3 The system area can be set when the "Advanced Setting" checkbox is selected.

*4 For the Q00UCPU, Q01UCPU, and Q02UCPU, "Multiple CPU Synchronous Startup Setting", “Online Module Change", and "Multiple CPU High Speed Transmission Area Setting" cannot be set.

*5 The consistency level differs depending on the CPU module used.
○ : For the Q00UCPU, Q01UCPU, and Q02UCPU
△ : For CPU modules other than the Q00UCPU, Q01UCPU, and Q02UCPU

Appendix 2 Comparison with a Single CPU System

This section describes comparison between a single CPU system and multiple CPU system.

(1) When a Basic model QCPU is used

Item		Single CPU system	Multiple CPU system	Reference
System configuration	Maximum number of extension levels	4 levels		Page 34, Section 3.1.1
	Maximum number of mountable I/O modules	24	25 - (Number of CPU modules)*1*2	
	Main base unit*3	Q3□B, Q3□SB, Q3□RB, Q3□DB		
	Extension base unit*3	Q5□B, Q6□B		
		Q6□RB		
	Extension cable	QC05B, QC06B, QC12B, QC30B, QC50B, QC100B		
	Overall extension cable distance	Within 13.2m		
	Power supply module*3	Q6□P, Q6□SP, Q6□RP		
Available module	Basic model QCPU	Function version A or later	Function version B	Page 34, Section 3.1.1, Page 42, Section 3.1.3
	I/O module	Function version A or later		
	Interrupt module	No function version restriction		
	Intelligent function module	Function version A or later	Function version B or later (Function version A or later for the QD62, QD62D, and QD62E)	
Available software package	GX Developer	Version 7 or later	Version 8 or later	Page 68, Section 3.4
	Other than above	The same version can be used in both single CPU systems and multiple CPU systems.		

*1 "Number of CPU modules" indicates the number set in "No. of PLC" of PLC parameter ("Multiple CPU Setting").

*2 When a module occupying two slots is mounted, the maximum number of mountable I/O modules is the number obtained by "25 - (Number of CPU modules + 1)".
When a module occupying three slots is mounted, the maximum number of mountable I/O modules is the number obtained by "25 - (Number of CPU modules + 2)".

*3 If a Motion CPU or PC CPU module is used in a multiple CPU system, the Q3□RB, Q6□RB, and Q6□RP cannot be used.

Item		Single CPU system	Multiple CPU system	Reference
Concept	Number of CPU modules and mounting position	Only 1 module in the CPU slot	3 modules in the CPU slot to slot 1	Page 63, Section 3.3.2
	I/O number assignment	Slot 0 is 00_H.	A slot on the right of the rightmost CPU module is 00_H.*1	Page 29, Section 2.2
	Restrictions on the number of mountable modules	The number of mountable modules differs depending on the CPU module type.	The number of mountable modules per system and the number of controllable modules per CPU module differ depending on the CPU module type.	Page 74, Section 3.5 (1) (c)
Access range	Access from CPU module(s) to other modules	All modules can be controlled.	Relations between CPU modules and other modules must be set in "Control PLC" of PLC parameter.	Page 107, CHAPTER 5
	Access from GOTs	Accessible		Manual for the GOT used
	Access with instructions using the link direct device	Accessible	Only control CPU is accessible.	Page 107, Section 5.2
	Access to CC-Link	Accessible	Only control CPU is accessible.	Manual for the CC-Link system master/local module used
	Access from peripherals	Accessible through an RS-232 cable or over network	Accessible through an RS-232 cable or over network. For access to the Motion CPU, PC CPU module, or C Controller module, refer to the relevant manual.	-
Clock function	Clock data used by intelligent function modules (such as the QD75)	Clock data of the Basic model QCPU is used.	Clock data of the Basic model QCPU (CPU No.1) is used.	Page 102, Section 4.4
Operation	Operation when a CPU module is reset	The entire system is reset by resetting the Basic model QCPU.	The entire system is reset by resetting the Basic model QCPU (CPU No.1). (Resetting CPU No.2 and No.3 individually is not allowed.)	Page 105, Section 4.6
	Operation when a stop error has occurred in a CPU module	The system stops.	If a stop error has occurred in the Basic model QCPU (CPU No.1), the system stops. ("MULTI CPU DOWN" (error code: 7000) occurs in CPU No.2 and No.3.) If a stop error has occurred in CPU No.2 or No.3, the operation depends on the parameter setting ("Operation Mode").	Page 105, Section 4.6

*1 When a CPU module occupying two slots is mounted, the slot on the right of the CPU module will be 10_H.
When a CPU module occupying three slots is mounted, the slot on the right of the CPU module will be 20_H.

Item		Single CPU system	Multiple CPU system	Reference
Communications among CPU modules	Communications by auto refresh using the CPU shared memory	Not supported	Basic model QCPU = 320 points, Motion CPU = 2048 points, C Controller module = 2048 points, PC CPU module = 2048 points, Total of all CPU modules: 4416 points	Page 125, Section 6.1.1
	Communications by programs using the CPU shared memory	Not supported	Data communications is performed by using the TO, S.TO, FROM instructions, and instructions using the cyclic transmission area device (U3En\G□).	Page 153, Section 6.1.3
	Communications between Basic model QCPU and Motion CPU	Not supported	Data communications is performed by using five motion dedicated instructions and three multiple CPU transmission dedicated instructions.	Page 163, Section 6.2, Page 165, Section 6.3.1
	Communications between Basic model QCPU and C Controller module/PC CPU module	Not supported	Data communications is performed by using the multiple CPU transmission dedicated instruction.	Page 167, Section 6.3.2
Scan time	Factors that increase scan time	• Writing data during RUN • Time reserved for communication processing	• Writing data during RUN • Time reserved for communication processing • Refresh processing among CPU modules in the multiple CPU system • Waiting time	Page 195, Appendix 4
Parameter	Parameters added for a multiple CPU system	Not supported	• Number of CPU modules ("Multiple CPU Setting") • Control PLC setting ("I/O Assignment") • Out-of-group I/O setting ("Multiple CPU Setting") • Operation mode when a stop error has occurred in a CPU module ("Multiple CPU Setting") • Communication area setting ("Refresh Setting") • Settings of some parameters must be the same for all the CPU modules while others can be set individually for each CPU module.	Page 83, Section 4.2.2, Page 173, Appendix 1
Precaution	AnS/A series module	Not supported		Page 191, Appendix 3

(2) When a High Performance model QCPU is used

Item		Single CPU system	Multiple CPU system	Reference
System configuration	Maximum number of extension levels	7 levels		Page 43, Section 3.2.1
	Maximum number of mountable I/O modules	64	65- (Number of CPU modules)*1*2	
	Main base unit*3	Q3□B, Q3□SB, Q3□RB, Q3□DB		
	Extension base unit*3*6	Q5□B, Q6□B, Q6□RB, QA1S5□B, QA1S6□B, QA1S6ADP+A1S5□B/A1S6□B, QA6□B, QA6ADP+A5□B/A6□B		
	Extension cable	QC05B, QC06B, QC12B, QC30B, QC50B, QC100B		
	Overall extension cable distance	Within 13.2m		
	Power supply module*3	Q6□P, Q6□SP, Q6□RP, A1S6□P, A6□P		
Available module	High Performance model QCPU	Function version A or later	Function version B	Page 43, Section 3.2.1, Page 53, Section 3.2.3
	I/O module	Function version A or later		
	Interrupt module	No function version restriction		
	Intelligent function module	Function version A or later	Function version B or later (Function version A or later for the QD62, QD62D, and QD62E.)	
Available software package	GX Developer	Version 4 or later	Version 6 or later	Page 68, Section 3.4
	GX Configurator-AD	SW0D5C-QADU 00A or later*4	SW0D5C-QADU 20C or later*4	
	GX Configurator-DA	SW0D5C-QDAU 00A or later*4	SW0D5C-QDAU 20C or later*4	
	GX Configurator-SC	SW0D5C-QSCU 00A or later*4	SW0D5C-QSCU 20C or later*4	
	GX Configurator-CT	SW0D5C-QCTU 00A or later*4	SW0D5C-QCTU 20C or later*4	
	Other than above	The same version can be used in both single CPU systems and multiple CPU systems.		
Concept	Number of CPU modules and mounting position	Only 1 module in the CPU slot	4 modules in the CPU slot to slot 2	Page 49, Section 3.2.2
	I/O number assignment	Slot 0 is 00_H.	A slot on the right of the rightmost CPU module is 00_H.*5	Page 29, Section 2.2
	Restrictions on number of mountable modules	The number of mountable modules differs depending on the CPU module type.	The number of mountable modules per system and the number of controllable modules per CPU module differ depending on the CPU module type.	Page 72, Section 3.5 (1) (b)

*1 "Number of CPU modules" indicates the number set in "No. of PLC" of PLC parameter ("Multiple CPU Setting").

*2 When a module occupying two slots is mounted, the maximum number of mountable I/O modules is the number obtained by "65 - (Number of CPU modules + 1)".
When a module occupying three slots is mounted, the maximum number of mountable I/O modules is the number obtained by "25 - (Number of CPU modules + 2)".

*3 If a Motion CPU or PC CPU module is used in a multiple CPU system, the Q3□RB, Q6□RB, and Q6□RP cannot be used.

*4 Available version differs for some intelligent function modules. (Manual for the intelligent function module used)

*5 When a CPU module occupying two slots is mounted, the slot on the right of the CPU module will be 10_H.
When a CPU module occupying three slots is mounted, the slot on the right of the CPU module will be 20_H.

*6 When the QA1S6ADP+A1S5□B/A1S6□B is used, the maximum number of extension base units is 1, and the maximum number of I/O modules that can be mounted is 20 minus the number of CPU modules. When the QA1S6ADP-S1+A1S5□B/A1S6□B is used, the maximum number of extension base units is 3, and the maximum number of I/O modules that can be mounted is 36 minus the number of CPU modules.

Item		Single CPU system	Multiple CPU system	Reference
Access range	Access from CPU module(s) to other modules	All modules can be controlled.	Relations between CPU modules and other modules must be set in "Control PLC" of PLC parameter.	Page 107, CHAPTER 5
	Access from GOTs	Accessible	A GOT can access a High Performance model QCPU of the specified CPU No.	Manual for the GOT used
	Access with instructions using the link direct device	Accessible	Only control CPU is accessible.	Page 107, Section 5.2
	Access to CC-Link	Accessible	Only control CPU is accessible.	Manual for the CC-Link system master/local module used
	Access from peripherals	Accessible through a USB cable/RS-232 cable or over network	Accessible through a USB cable/RS-232 cable or over network. For access to the Motion CPU, PC CPU module, or C Controller module, refer to the relevant manual.	-
Clock function	Clock data used by intelligent function modules (such as the QD75)	Clock data of the High Performance model QCPU is used.	Clock data of the High Performance model QCPU (CPU No.1) is used.	Page 102, Section 4.4
Operation	Operation when a CPU module is reset.	The entire system is reset by resetting the High Performance model QCPU.	The entire system is reset by resetting the High Performance model QCPU (CPU No.1). (Resetting CPU No.2 to No.4 individually is not allowed.)	Page 105, Section 4.6
	Operation when a stop error has occurred in a CPU module	The system stops.	If a stop error has occurred in the High Performance model QCPU (CPU No.1), the system stops. ("MULTI CPU DOWN" (error code: 7000) occurs in CPU No.2 to No.4.) If a stop error has occurred in CPU No.2 to No.4, the operation depends on the parameter setting ("Operation Mode").	Page 105, Section 4.6
Communications among CPU modules	Communications by auto refresh using the CPU shared memory	Not supported	Total of 4 Settings per CPU module: up to 2K words, Total of all CPU modules: 8K words	Page 125, Section 6.1.1
	Communications by programs using the CPU shared memory	Not supported	Data communications is performed by using the S.TO, FROM instructions, and instructions using the cyclic transmission area device (U3En\G□).	Page 153, Section 6.1.3
	Communications between High Performance model QCPU and Motion CPU	Not supported	Data communications is performed by using five motion dedicated instructions and three multiple CPU transmission dedicated instructions.	Page 163, Section 6.2, Page 165, Section 6.3.1
	Communication between High Performance model QCPU and C Controller module/PC CPU module	Not supported	Data communications is performed by using the multiple CPU transmission dedicated instruction.	Page 167, Section 6.3.2

Item		Single CPU system	Multiple CPU system	Reference
Scan time	Factors that increase scan time	• Writing data during RUN • Time reserved for communication processing	• Writing data during RUN • Time reserved for communication processing • Refresh processing among CPU modules in the multiple CPU system • Waiting time	Page 195, Appendix 4
Parameter	Parameters added for a multiple CPU system	Not supported	• Number of CPU modules ("Multiple CPU Setting") • Control PLC setting ("I/O Assignment") • Out-of-group I/O setting ("Multiple CPU Setting") • Operation mode when a stop error has occurred in a CPU module ("Multiple CPU Setting") • Communication area setting ("Refresh Setting") • Settings of some parameters must be the same for all the CPU modules while others can be set individually for each CPU module.	Page 83, Section 4.2.2, Page 173, Appendix 1
Precaution	AnS/A series module	Supported	Supported only when a High Performance model QCPU is set as a control CPU.	Page 191, Appendix 3

(3) When a Process CPU is used.

Item		Single CPU system	Multiple CPU system	Reference
System configuration	Maximum number of extension levels	7 levels		Page 43, Section 3.2.1
	Maximum number of mountable I/O modules	64	65 - (Number of CPU modules)*1*2	
	Main base unit*3	Q3□B, Q3□RB, Q3□DB		
	Extension base unit*3	Q5□B, Q6□B, Q6□RB		
	Extension cable	QC05B, QC06B, QC12B, QC30B, QC50B, QC100B		
	Overall extension cable distance	Within 13.2m		
	Power supply module*3	Q6□P, Q6□RP		
Available module	Process CPU	No function version restriction		Page 43, Section 3.2.1, Page 53, Section 3.2.3
	I/O module	Function version A or later		
	Interrupt module	No function version restriction		
	Intelligent function module	Function version A or later	Function version B or later (Function version A or later for the QD62, QD62D, and QD62E.)	
Available software package	GX Works2, GX Developer, PX Developer, GX Configurator	The same version can be used in both single CPU systems and multiple CPU systems.		Page 68, Section 3.4
Concept	Number of CPU modules and mounting position	Only 1 module in the CPU slot	4 modules in the CPU slot to slot 2	Page 49, Section 3.2.2
	I/O number assignment	Slot 0 is 00_H.	A slot on the right of the rightmost CPU module is 00_H.*4	Page 29, Section 2.2
	Restrictions on the number of mountable modules	The number of mountable modules differs depending on the CPU module type.	The number of mountable modules per system and the number of controllable modules per CPU module differ depending on the CPU module type.	Page 72, Section 3.5 (1) (b)

*1 "Number of CPU modules" indicates the number set in "No. of PLC" of PLC parameter ("Multiple CPU Setting").

*2 When a module occupying two slots is mounted, the maximum number of mountable I/O modules is the number obtained by "25 - (Number of CPU modules + 1)".
When a module occupying three slots is mounted, the maximum number of mountable I/O modules is the number obtained by "25 - (Number of CPU modules + 2)".

*3 If a Motion CPU or PC CPU module is used in a multiple CPU system, the Q3□RB, Q6□RB, and Q6□RP cannot be used.

*4 When a CPU module occupying two slots is mounted, the slot on the right of the CPU module will be 10_H.
When a CPU module occupying three slots is mounted, the slot on the right of the CPU module will be 20_H.

Item		Single CPU system	Multiple CPU system	Reference
Access range	Access from CPU module(s) to other modules	All modules can be controlled.	Relations between CPU modules and other modules must be set in "Control PLC" of PLC parameter.	Page 107, CHAPTER 5
	Access from GOTs	Accessible	A GOT can access a Process CPU of the specified CPU No.	Manual for the GOT used
	Access with instructions using the link direct device	Accessible	Only control CPU is accessible.	Page 107, Section 5.2
	Access to CC-Link	Accessible	Only control CPU is accessible.	Manual for the CC-Link system master/local module used
	Access from peripherals	Accessible through a USB cable/RS-232 cable or over network	Accessible through a USB cable/RS-232 cable or over network. For access to the Motion CPU, PC CPU module, or C Controller module, refer to the relevant manual.	-
Clock function	Clock data used by intelligent function modules (such as the QD75)	Clock data of the Process CPU is used.	Clock data of the Process CPU (CPU No.1) is used.	Page 102, Section 4.4
Operation	Operation when a CPU module is reset.	The entire system is reset by resetting the Process CPU.	The entire system is reset by resetting the Process CPU (CPU No.1). (Resetting CPU No.2 to No.4 individually is not allowed.)	Page 105, Section 4.6
	Operation when a stop error has occurred in a CPU module	The system stops.	If a stop error has occurred in the Process CPU (CPU No.1), the system stops. ("MULTI CPU DOWN" (error code: 7000) occurs in CPU No.2 to No.4.) If a stop error has occurred in CPU No.2 to No.4, the operation depends on the parameter setting ("Operation Mode").	Page 105, Section 4.6
Communications among CPU modules	Communications by auto refresh using the CPU shared memory	Not supported	Total of 4 Settings per CPU module: up to 2K words, Total of all CPU modules: 8K words	Page 125, Section 6.1.1
	Communications by programs using the CPU shared memory	Not supported	Data communications is performed by using the S.TO, FROM instructions, and instructions using the cyclic transmission area device (U3En\G□).	Page 153, Section 6.1.3
	Communications between Process CPU and Motion CPU	Not supported	Data communications is performed by using five motion dedicated instructions and three multiple CPU transmission dedicated instructions.	Page 163, Section 6.2, Page 165, Section 6.3.1
	Communications between Process CPU and C Controller module/PC CPU module	Not supported	Data communications is performed by using the multiple CPU transmission dedicated instruction.	Page 167, Section 6.3.2

Item		Single CPU system	Multiple CPU system	Reference
Scan time	Factors that increase scan time	• Writing data during RUN • Time reserved for communication processing	• Writing data during RUN • Time reserved for communication processing • Refresh processing among CPU modules in a multiple CPU system • Waiting time	Page 195, Appendix 4
Parameter	Parameters added for multiple CPU systems	Not supported	• Number of CPU modules ("Multiple CPU Setting") • Control PLC setting ("I/O Assignment") • Out-of-group I/O setting ("Multiple CPU Setting") • Operation mode when a stop error has occurred in a CPU module ("Multiple CPU Setting") • Communication area setting ("Refresh Setting") • Settings of some parameters must be the same for all the CPU modules while others can be set individually for each CPU module.	Page 83, Section 4.2.2, Page 173, Appendix 1
Precaution	AnS/A series module	Not supported		Page 191, Appendix 3

(4) When a Universal model QCPU is used

Item		Single CPU system	Multiple CPU system	Reference
System configuration	Maximum number of extension levels	7 levels (Q00UCPU, Q01UCPU, or Q02UCPU: 4 levels)		Page 55, Section 3.3.1
	Maximum number of mountable I/O modules	64 (Q00UCPU or Q01UCPU: 24, Q02CPU: 36)	65 - (Number of CPU modules)*1*2 (Q00UCPU or Q01UCPU: 25 - (Number of CPU modules), Q02UCPU: 37 - (Number of CPU modules))	
	Main base unit*3*6	Q3B, Q3SB, Q3RB, Q3DB		
	Extension base unit*3*4*5	Q5□B, Q6□B, Q6□RB, QA1S5□B, QA1S6□B, QA1S6ADP+A1S5□B/A1S6□B, QA6□B, QA6ADP+A5□B/A6□B		
	Extension cable	QC05B, QC06B, QC12B, QC30B, QC50B, QC100B		
	Overall extension cable distance	Within 13.2m		
	Power supply module*3	Q6□P, Q6□SP, Q6□RP		
Available module	Universal model QCPU	No function version restriction		Page 55, Section 3.3.1, Page 67, Section 3.3.3
	I/O module	Function version A or later		
	Interrupt module	No function version restriction		
	Intelligent function module	Function version A or later	Function version B or later (Function version A or later for the QD62, QD62D, and QD62E)	
Available software package	GX Works2, PX Developer*5, GX Configurator	The same version can be used in both single CPU systems and multiple CPU systems.		Page 68, Section 3.4

*1 "Number of CPU modules" indicates the number set in "No. of PLC" of PLC parameter ("Multiple CPU Setting").

*2 When a module occupying two slots is mounted, the maximum number of mountable I/O modules is the number obtained by "65 - (Number of CPU modules + 1)".
When a module occupying three slots is mounted, the maximum number of mountable I/O modules is the number obtained by "65 - (Number of CPU modules + 2)".

*3 If a Motion CPU or PC CPU module is used in a multiple CPU system, the Q3□RB, Q6□RB, and Q6□RP cannot be used.

*4 AnS/A series-compatible modules can be used with a Universal model QCPU with a serial number (first five digits) of "13102" or later. (Except for the QnUDPVCPU)

*5 PX Developer can be used with the QnUDPVCPU.

*6 If the QnUDPVCPU is used, the Q3□SB cannot be used.

*7 When the QA1S6ADP+A1S5□B/A1S6□B is used, the maximum number of extension base units is 1, and the maximum number of I/O modules that can be mounted is 20 minus the number of CPU modules. When the QA1S6ADP-S1+A1S5□B/A1S6□B is used, the maximum number of extension base units is 3, and the maximum number of I/O modules that can be mounted is 36 minus the number of CPU modules.

Item		Single CPU system	Multiple CPU system	Reference
Concept	Number of CPU modules and mounting position	Only 1 module in the CPU slot	4 modules in the CPU slot to slot 2	Page 63, Section 3.3.2
	I/O number assignment	Slot 0 is 00_H.	A slot on the right of the rightmost CPU module is 00_H.*1	Page 29, Section 2.2
	Restrictions on the number of mountable modules	The number of mountable modules differs depending on the CPU module type.	The number of mountable modules per system and the number of controllable modules per CPU module differ depending on the CPU module type.	Page 74, Section 3.5 (1) (c)
Access range	Access from CPU module(s) to other modules	All modules can be controlled.	Relations between CPU modules and other modules must be set in "Control PLC" of PLC parameter.	Page 107, CHAPTER 5
	Access from GOTs	Accessible	A GOT can access a Universal model QCPU of the specified CPU No.	Manual for the GOT used
	Access with instructions using the link direct device	Accessible	Only control CPU is accessible.	Page 107, Section 5.2
	Access to CC-Link	Accessible	Only control CPU is accessible.	Manual for the CC-Link system master/local used
	Access from peripherals	Accessible through a USB cable/RS-232 cable/Ethernet cable or over network.	Accessible through a USB cable/RS-232 cable/Ethernet cable or over network. For access to the Motion CPU, PC CPU module, or C Controller module, refer to the relevant manual.	-
Clock function	Clock data used by CPU No.2 to No.4	Not supported	Clock data of the Universal model QCPU (CPU No.1) (except the Q00UCPU, Q01UCPU, and Q02UCPU) is used.*2	Page 102, Section 4.4
	Clock data used by intelligent function modules (such as the QD75)	Clock data of the Universal model QCPU is used.	Clock data of the Universal model QCPU (CPU No.1) is used.	

*1 When a CPU module occupying two slots is mounted, the slot on the right of the CPU module will be 10_H.
When a CPU module occupying three slots is mounted, the slot on the right of the CPU module will be 20_H.

*2 When a Universal model QCPU (except the Q00UCPU, Q01UCPU, and Q02UCPU), Motion CPU (Q172DCPU(-S1), Q173DCPU(-S1), Q172DSCPU, or Q173DSCPU), or C Controller module (Q12DCCPU-V, Q24DHCCPU-V, Q24DHCCPU-VG, Q24DHCCPU-LS, or Q26DHCCPU-LS) is used as any of CPU No.2 to No.4, clock data in CPU No.1 can be used.

Item		Single CPU system	Multiple CPU system	Reference
Operation	Operation when a CPU module is reset.	The entire system is reset by resetting the Universal model QCPU.	The entire system is reset by resetting the Process CPU (CPU No.1). (Resetting CPU No.2 to No.4 individually is not allowed.)	Page 105, Section 4.6
	Operation when a stop error has occurred in a CPU module	The system stops.	If a stop error has occurred in the Process CPU (CPU No.1), the system stops. ("MULTI CPU DOWN" (error code: 7000) occurs in CPU No.2 to No.4.) If a stop error has occurred in CPU No.2 to No.4, the operation depends on the parameter setting ("Operation Mode").	Page 105, Section 4.6
	Multiple CPU system synchronized startup	Not supported	Whether to synchronize the startup of CPU modules in the multiple CPU system or not can be set. (The default is set to be synchronized.)	Page 171, Section 6.5
Communications between CPU modules	Communications by auto refresh using the CPU shared memory	Not supported	Total of 4 Settings per CPU module: up to 2K words, Total of all CPU modules: 8K words	Page 125, Section 6.1.1
	Communications by auto refresh using the multiple CPU high speed transmission area*1	Not supported	Total memory capacity used by all CPU modules: 2 CPU modules: 14K words, 3 CPU modules: 13K words, 4 CPU modules: 12K words	Page 138, Section 6.1.2
	Communications by programs using the CPU shared memory	Not supported	Data communications is performed by using the TO, FROM instructions, and instructions using the cyclic transmission area device (U3En\G□).	Page 153, Section 6.1.3
	Communications between Universal model QCPU and Motion CPU	Not supported	Data communications is performed by using five motion dedicated instructions and three multiple CPU transmission dedicated instructions.	Page 163, Section 6.2, Page 165, Section 6.3.1
	Communications between Universal model QCPU and C Controller module/PC CPU module	Not supported	Data communications is performed by using the multiple CPU transmission dedicated instruction.	Page 167, Section 6.3.2
	Communications between Universal model QCPUs	Not supported	Data communications is performed by using two multiple CPU high-speed transmission dedicated instructions.	Page 168, Section 6.3.3
Scan time	Factors that increase scan time	• Writing data during RUN • Time reserved for communication processing	• Writing data during RUN • Time reserved for communication processing • Refresh processing among CPU modules in a multiple CPU system • Waiting time	Page 195, Appendix 4

*1 When the Q00UCPU, Q01UCPU, or Q02UCPU is used as CPU No.1, this type of communications cannot be performed.

Item		Single CPU system	Multiple CPU system	Reference
Parameter	Parameters added for multiple CPU systems	Not supported	• Number of CPU modules ("Multiple CPU Setting") • Control PLC setting ("I/O Assignment") • Out-of-group I/O setting ("Multiple CPU Setting") • Operation mode when a stop error has occurred in a CPU module ("Multiple CPU Setting") • Multiple CPU synchronous startup ("Multiple CPU Setting") • Multiple CPU high speed transmission area setting ("Multiple CPU Setting")*1 • Communication area setting ("Refresh Setting") • Settings of some parameters must be the same for all the CPU modules while others can be set individually for each CPU module.	Page 83, Section 4.2.2,Page 173, Appendix 1
Caution	AnS/A series module*2	Supported	Supported only when a Universal model QCPU is set as a control CPU.	Page 191, Appendix 3

*1 When the Q00UCPU, Q01UCPU, or Q02UCPU is used as CPU No.1, this parameter cannot be set.

*2 AnS/A series-compatible modules can be used with a Universal model QCPU with a serial number (first five digits) of "13102" or later. (Except for the QnUDPVCPU)

Appendix 3 Precautions for Using AnS/A Series Modules

(1) Multiple CPU system configuration for using AnS/A series modules

AnS/A series modules can be used in a multiple CPU system configuration where all of the following conditions are met.

(a) CPU No.1

The following QCPU must be used.

- Universal model QCPU with a serial number (first five digits) of "13102" or later (Except QnUDPVCPU)
- High Performance model QCPU

(b) CPU No.2 to No.4

The following CPU module must be used.

- Universal model QCPU with a serial number (first five digits) of "13102" or later (Except QnUDPVCPU)
- High Performance model QCPU
- Motion CPU
- C Controller module
- PC CPU module

AnS/A series modules cannot be used in the system using the system configuration other than the above.

(2) Control CPU setting

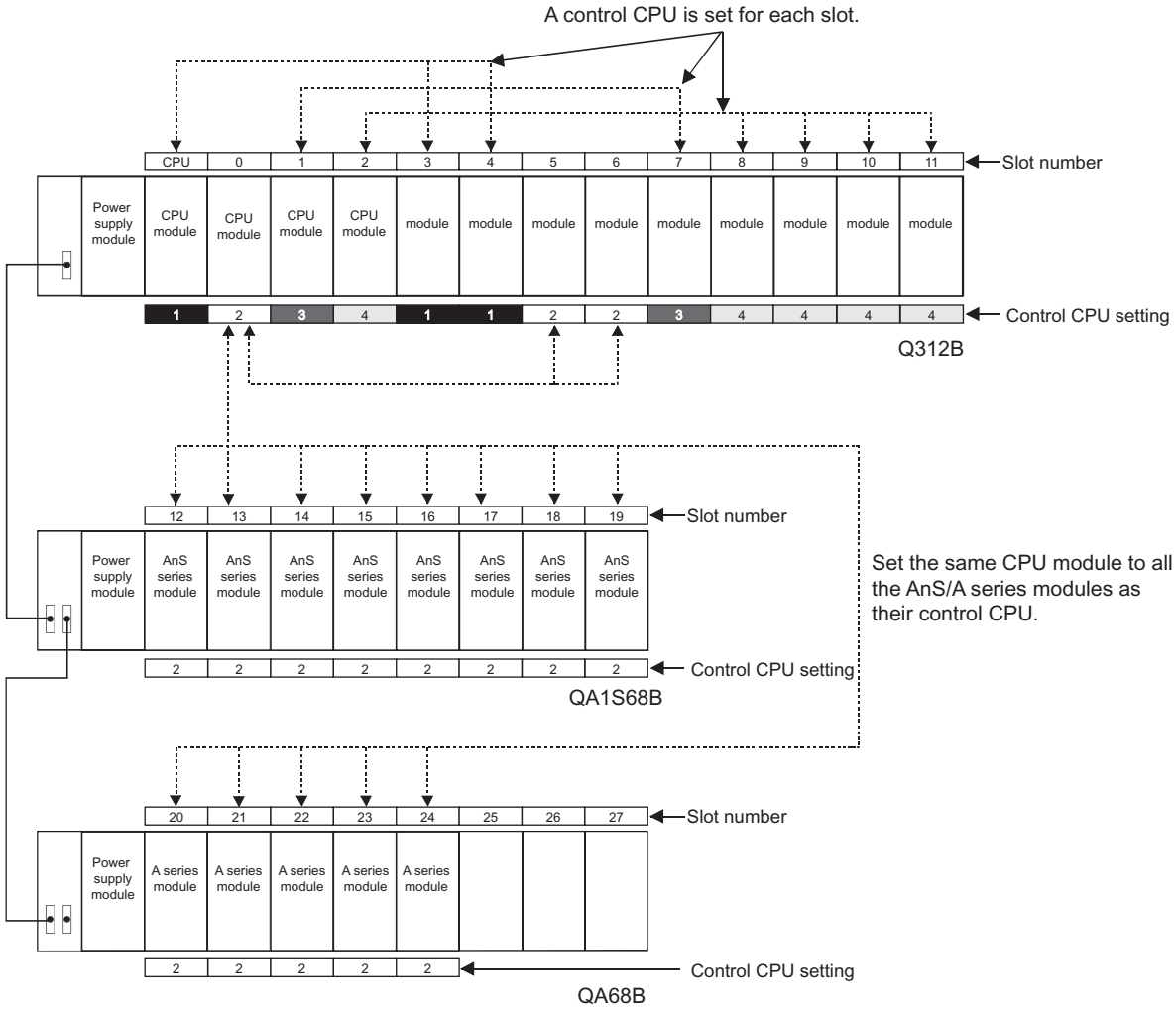
Set either of the following QCPUs as a control CPU of AnS/A series modules.

- Universal model QCPU with a serial number (first five digits) of "13102" or later (Except QnUDPVCPU)
- High Performance model QCPU

Note that only one CPU module can be set as a control CPU.

Ex. When CPU No.2 is set as a control CPU

Set CPU No.2 as the control CPU of all slots where AnS/A series modules are mounted. If a different CPU No. is set as a control CPU for any of the AnS/A series modules, "PARAMETER ERROR" (error code: 3009) will occur and the multiple CPU system will not start.



The control CPU setting shown above indicates the following:

CPU modules 1 to 4:	CPU number
Other than CPU modules:	Control CPU number

(3) Access ranges of controlled and non-controlled modules

Access ranges of the controlled and non-controlled modules in a multiple CPU system is shown below.

○: Accessible ×: Inaccessible

Access target		Controlled module	Non-controlled module ("All CPUs Can Read All Inputs")	
			Disabled (not checked)	Enabled (checked)
Input (X)		○	×	×
Output (Y)	Read	○	×	×
	Write	○	×	×
Buffer memory	Read	○	×	×
	Write	○	×	×

(4) Precautions

(a) Accessible device ranges

When the following AnS/A series modules are used, accessible device ranges are restricted.

- A1SJ71J92-S3, AJ71J92-S3 type JEMANET interface module
- A1SD51S, AD51-S3, AD51H-S3 type intelligent communication module
- A1SJ71AP23Q, A1SJ71AR23Q, A1SJ71AT23BQ type MELSECNET local station data link module

Device	Accessible device range
Input (X), Output (Y)	X/Y0 to X/Y7FF
Internal relay (M), Latch relay (L)	M/L0 to M/L8191
Link relay (B)	B0 to BsFFF
Timer (T)	T0 to T2047
Counter (C)	C0 to C1023
Data register (D)	D0 to D6143
Link register (W)	W0 to WFFF
Annunciator (F)	F0 to F2047

(b) Unavailable modules

The following modules cannot be used.

Product	Model name
MELSECNET/10 network module	A1SJ71LP21, A1SJ71BR11, A1SJ71QLP21, A1SJ71QLP21S, A1SJ71QLP21GE, A1SJ71QBR11, AJ71LP21, AJ71LP21G, AJ71BR11, AJ71LR21, AJ71QLP21, AJ71QLP21S, AJ71QLP21G, AJ71QBR11, AJ71QLR21
MELSECNET (II), /B data link module	A1SJ71AP21, A1SJ71AR21, A1SJ71AT21B, AJ71AP21, AJ71AP21-S3, AJ71AR21, AJ71AT21B
Ethernet interface module	A1SJ71QE71-B2-S3(-B5-S3), A1SJ71E71-B2-S3(-B5-S3), AJ71QE71N-B2(-B5T), AJ71E71N-B2(-B5T)
Serial communication module, computer link module	A1SJ71QC24(N), A1SJ71UC24-R2(-PRF), AJ71QC24(N), AJ71QC24N-R2(-R4), A1SJ71UC24, AJ71UC24
Computer link/multidrop link module	A1SJ71UC24-R4*1
CC-Link master/local module	A1SJ61QBT11, A1SJ61BT11, AJ61QBT11, AJ61BT11
ME-NET interface module	A1SJ71ME81, AJ71ME81

*1 Only the multidrop link function is supported. The computer link and printer functions are not supported.

(c) Modules that require program modification

Dedicated instructions for the following special function modules cannot be used. Modify the program using the FROM/TO instructions.

Product	Model name
High-speed counter module	A1SD61, A1SD62, A1SD62D(-S1), A1SD62E, AD61, AD61S1
MELSECNET/MINI-S3	A1SJ71PT32-S3, A1SJ71T32-S3, AJ71PT32-S3, AJ71T32-S3
Positioning module	A1SD75P1-S3(P2-S3/P3-S3), AD75M1(M2/M3), AD75P1-S3(P2-S3/P3-S3)
ID module	A1SJ71ID1-R4, A1SJ71ID2-R4, AJ71ID1-R4, AJ71ID2-R4

Appendix 4 Processing Time

Appendix 4.1 Concept of scan time

The concept of scan time in a multiple CPU system is the same as that in a single CPU system.
This section describes how to calculate the processing time when a multiple CPU system is configured.

(1) I/O refresh time

For the calculating formula of I/O refresh time, refer to the following.

User's Manual (Function Explanation, Program Fundamentals) for the CPU module used

The I/O refresh time increases by the time obtained by the following calculation when more than one CPU module simultaneously accesses I/O modules and intelligent function modules through the bus .

$$\text{(Extended time)} = \frac{\text{(Number of input points + Number of output points)}}{16} \times N3 \times \text{(Number of other CPU modules) (μs)}$$

Use the following value for N3.

QCPU	N3	
	System with a main base unit only	System including extension base unit(s)
Q00CPU, Q01CPU	8.7μs	21μs
Q02(H)CPU, Q06HCPU, Q12HCPU, Q25HCPU		
Q02PHCPU, Q06PHCPU, Q12PHCPU, Q25PHCPU		
Q00UCPU, Q01UCPU, Q02UCPU, Q03UD(E)CPU, Q04UD(E)HCPU, Q06UD(E)HCPU, Q10UD(E)HCPU, Q13UD(E)HCPU, Q20UD(E)HCPU, Q26UD(E)HCPU, Q50UDEHCPU, Q100UDEHCPU		
Q03UDVCPU, Q04UDVCPU, Q04UDPVCPU, Q06UDVCPU, Q06UDPVCPU, Q13UDVCPU, Q13UDPVCPU, Q26UDVCPU, Q26UDPVCPU		

(2) Total instruction execution time

For the processing time of the multiple CPU system dedicated instructions and the processing time of instructions whose processing times differ between in a single CPU system and a multiple CPU system, refer to the following.

MELSEC-Q/L Programming Manual (Common Instruction)

(3) Common processing time

In a multiple CPU system, the common processing time increases as shown below.

QCPU	Common processing time
Q00CPU, Q01CPU	(0.05 to 0.13) × (Number of other CPU modules) ms
Q02CPU	0.02ms
Q02HCPU, Q06HCPU, Q12HCPU, Q25HCPU	0.03ms
Q02PHCPU, Q06PHCPU, Q12PHCPU, Q25PHCPU	
Q00UCPU, Q01UCPU, Q02UCPU, Q03UD(E)CPU, Q04UD(E)HCPU, Q06UD(E)HCPU, Q10UD(E)HCPU, Q13UD(E)HCPU, Q20UD(E)HCPU, Q26UD(E)HCPU, Q50UDEHCPU, Q100UDEHCPU	0.02ms
Q03UDVCPU, Q04UDVCPU, Q04UDPVCPU, Q06UDVCPU, Q06UDPVCPU, Q13UDVCPU, Q13UDPVCPU, Q26UDVCPU, Q26UDPVCPU	

Appendix 4.2 Factors that increase scan time

The processing time in a multiple CPU system increases from that in a single CPU system when the following functions are used.
When any of the following functions is used, add the time values described in this section to the values calculated on Page 195, Appendix 4.1.

- Auto refresh of the CPU shared memory (including the multiple CPU high speed transmission function)
- Refresh of CC-Link IE and MELSECNET/H
- Auto refresh of CC-Link

(1) Auto refresh of the CPU shared memory (including the multiple CPU high speed transmission function)

(a) Auto refresh time of the CPU shared memory

This is the time required for executing refresh set in "Communication Area Setting (Refresh Setting)" and "Multiple CPU High Speed Transmission Area Setting" of PLC parameter ("Multiple CPU Setting"). The value is the total amount of time required for the CPU module to write data to its own CPU shared memory and read data from the CPU shared memory of other CPU modules.
The time value needs to be added when refresh is set in "Communication Area Setting (Refresh Setting)" and "Multiple CPU High Speed Transmission Area Setting" of PLC parameter ("Multiple CPU Setting").

(b) Calculating formula

The time value is obtained by the following calculation.

- For the Basic model QCPU

(Auto refresh time)
= (N1 + (Number of send word points) × N2) +
(N3 + (Number of other CPU modules) × N4 + (Number of receive word points) × N5) (μs)

The number of receive word points is the sum of the number of word points sent by other CPU modules.

Ex. When the number of CPU modules is 3 and the host CPU is CPU No.1
The number of receive word points will be the sum of the number of word points sent by CPU No.2 and No.3.

Use the following values for N1 to N5.

Basic model QCPU	N1	N2	N3	N4	N5
Q00CPU	63μs	1.13μs	63μs	161μs	0.88μs
Q01CPU	57μs	1.03μs	57μs	146μs	0.80μs

• For the High Performance model QCPU and Process CPU

(Auto refresh time) = (N1 + (Number of receive word points) × N2) × (Number of other CPU modules)
+ (N3 + (Number of send word points) × N4) (μs)

The number of receive word points is the sum of the number of word points sent by other CPU modules.

Ex. When the number of CPU modules is 4 and the host CPU is CPU No.1
The number of receive word points will be the sum of the number of word points sent by CPU No.2 to No.4.

Use the following values for N1 to N4.

High Performance model QCPU, Process CPU	N1	N2	N3	N4
Q02CPU	82μs	0.52μs	106μs	0.17μs
Q02HCPU, Q06HCPU, Q12HCPU, Q25HCPU	27μs	0.44μs	27μs	0.08μs
Q02PHCPU, Q06PHCPU, Q12PHCPU, Q25PHCPU				

• For the Universal model QCPU

(Auto refresh time)

= (N1 + (Number of send word points) × N2) +
(N3 + (Number of other CPU modules) × N4 + (Number of receive word points) × N5) (μs)

The number of receive word points is the sum of the number of word points sent by other CPU modules.

Ex. When the number of CPU modules is 4 and the host CPU is CPU No.1
The number of receive word points will be the sum of the number of word points sent by CPU No.2 to No.4.

For the auto refresh using the multiple CPU high speed transmission area, use the following values for N1 to N5.

Universal model QCPU	N1	N2	N3	N4	N5
Q00UCPU, Q01UCPU, Q02UCPU	-	-	-	-	-
Q03UD(E)CPU	6μs	0.207μs	2μs	9μs	0.393μs
Q04UD(E)HCPU, Q06UD(E)HCPU, Q10UD(E)HCPU, Q13UD(E)HCPU, Q20UD(E)HCPU, Q26UD(E)HCPU, Q50UDEHCPU, Q100UDEHCPU	6μs	0.183μs	2μs	9μs	0.327μs
Q03UDVCPU, Q04UDVCPU, Q04UDPVCPU, Q06UDVCPU, Q06UDPVCPU, Q13UDVCPU, Q13UDPVCPU, Q26UDVCPU, Q26UDPVCPU	6μs	0.183μs	1μs	4μs	0.256μs

For the auto refresh using the CPU shared memory, use the following values for N1 to N5.

Universal model QCPU	N1	N2	N3	N4	N5
Q00UCPU, Q01UCPU, Q02UCPU	34μs	0.155μs	120μs	30μs	0.420μs
Q03UD(E)CPU	9μs	0.162μs	28μs	21μs	0.410μs
Q04UD(E)HCPU, Q06UD(E)HCPU, Q10UD(E)HCPU, Q13UD(E)HCPU, Q20UD(E)HCPU, Q26UD(E)HCPU, Q50UDEHCPU, Q100UDEHCPU	8μs	0.132μs	25μs	20μs	0.410μs
Q03UDVCPU, Q04UDVCPU, Q04UDPVCPU, Q06UDVCPU, Q06UDPVCPU, Q13UDVCPU, Q13UDPVCPU, Q26UDVCPU, Q26UDPVCPU	4μs	0.105μs	12μs	10μs	0.410μs

(c) When auto refresh is executed by another CPU module during auto refresh processing

The auto refresh time increases by the time obtained by the following calculation.

- For the Basic model QCPU

(Extended time) = 4 × (Number of receive word points) × N6 × (Number of other CPU modules) (μs)

Use the following value for N6.

Basic model QCPU	N6	
	System with a main base unit only	System including extension base unit(s)
Q00CPU, Q01CPU	0.54μs	1.30μs

- For the High Performance model QCPU, Process CPU, and Universal model QCPU

(Extended time) = (Number of send/receive word points) × N5
× (Number of other CPU modules) (μs)

Use the following value for N5.

High Performance model QCPU, Process CPU, Universal model QCPU	N5	
	System with a main base unit only	System including extension base unit(s)
Q02(H)CPU, Q06HCPU, Q12HCPU, Q25HCPU	0.54μs	1.30μs
Q02PHCPU, Q06PHCPU, Q12PHCPU, Q25HCPU		
Q00UCPU, Q01UCPU, Q02UCPU, Q03UD(E)CPU, Q04UD(E)HCPU, Q06UD(E)HCPU, Q10UD(E)HCPU, Q13UD(E)HCPU, Q20UD(E)HCPU, Q26UD(E)HCPU, Q50UDEHCPU, Q100UDEHCPU		
Q03UDVCPU, Q04UDVCPU, Q04UDPVCPU, Q06UDVCPU, Q06UDPVCPU, Q13UDVCPU, Q13UDPVCPU, Q26UDVCPU, Q26UDPVCPU		

(2) Refresh of CC-Link IE and MELSECNET/H

(a) Refresh time of CC-Link IE and MELSECNET/H

This is the time required for executing refresh between a QCPU and a CC-Link IE module or MELSECNET/H module. For each refresh time, refer to the following.

Reference manual for each network module used

(b) Calculating formula

In a multiple CPU system, if refresh is executed by a network module controlled by another CPU module during refresh processing, the refresh time increases by the time obtained by the following calculation.

• For the Basic model QCPU

(Extended time) = 4 × (Number of send/receive word points) × N6 × (Number of other CPU modules) (μs)

The number of send/receive word points is the total points of the following transfer data.

- Link refresh data: $\frac{(LB + LX + LY + SB)}{16} + LW + SW$

Use the following value for N6.

Basic model QCPU	N6	
	System with a main base unit only	System including extension base unit(s)
Q00CPU, Q01CPU	0.54μs	1.30μs

• For the High Performance model QCPU, Process CPU, and Universal model QCPU

(Extended time) = (Number of send/receive word points) × N5 × (Number of other CPU modules) (μs)

The number of send/receive word points is the total points of the following transfer data.

- Link refresh data: $\frac{(LB + LX + LY + SB)}{16} + LW + SW$
- Data transferred to a file register in a memory card/SD memory card: $\frac{(LB + LX + LY + SB)}{16} + LW + SW$
- Interlink data transfer: $\left(\frac{LB}{16} + LW\right) \times 2$

Use the following value for N5.

High Performance model QCPU, Process CPU, Universal model QCPU	N5	
	System with a main base unit only	System including extension base unit(s)
Q02(H)CPU, Q06HCPU, Q12HCPU, Q25HCPU	0.54μs	1.30μs
Q02PHCPU, Q06PHCPU, Q12PHCPU, Q25HCPU		
Q00UCPU, Q01UCPU, Q02UCPU, Q03UD(E)CPU, Q04UD(E)HCPU, Q06UD(E)HCPU, Q10UD(E)HCPU, Q13UD(E)HCPU, Q20UD(E)HCPU, Q26UD(E)HCPU, Q50UDEHCPU, Q100UDEHCPU		
Q03UDVCPU, Q04UDVCPU, Q04UDPVCPU, Q06UDVCPU, Q06UDPVCPU, Q13UDVCPU, Q13UDPVCPU, Q26UDVCPU, Q26UDPVCPU		

(3) Auto refresh of CC-Link

(a) Auto refresh time of CC-Link

This is the time required for executing refresh between a QCPU and a CC-Link master/local module.
For details, refer to the following.

MELSEC-Q CC-Link System Master/Local Module User's Manual

(b) Calculating formula

In a multiple CPU system, when auto refresh is requested by a CC-Link module controlled by another CPU module during auto refresh processing, the auto refresh time increases by the time obtained by the following calculation.

(Extended time) = (Number of send/receive word points) × N5 × (Number of other CPU modules) (μs)

The number of send/receive word points is the total points of the following transfer data.

- Link refresh data: $\frac{(RX + RY + SB)}{16}$ + SW

Use the following value for N5.

QCPU	N5	
	System with a main base unit only	System including extension base unit(s)
Q00CPU, Q01CPU	0.54μs	1.30μs
Q02(H)CPU, Q06HCPU, Q12HCPU, Q25HCPU		
Q02PHCPU, Q06PHCPU, Q12PHCPU, Q25PHCPU		
Q00UCPU, Q01UCPU, Q02UCPU, Q03UD(E)CPU, Q04UD(E)HCPU, Q06UD(E)HCPU, Q10UD(E)HCPU, Q13UD(E)HCPU, Q20UD(E)HCPU, Q26UD(E)HCPU, Q50UDEHCPU, Q100UDEHCPU		
Q03UDVCPU, Q04UDVCPU, Q04UDPVCPU, Q06UDVCPU, Q06UDPVCPU, Q13UDVCPU, Q13UDPVCPU, Q26UDVCPU, Q26UDPVCPU		

Appendix 4.3 Reducing processing time

(1) Multiple CPU system processing

CPU modules access I/O modules and intelligent function modules through a bus (base unit pattern or extension cable). Note that only one CPU module can use the bus at a time.

If more than one CPU module attempts to use the bus simultaneously, the CPU module attempted access later is placed in Standby status until the processing of the first CPU module is completed.

In a multiple CPU system, this waiting time will cause delay in input and output, and consequently the scan time increases.

(2) Maximum waiting time

In a multiple CPU system, the waiting time of the host CPU will reach the maximum when:

- The maximum number of CPU modules allowed in the system is used.
- An extension base unit is used.
- An intelligent function module on an extension base unit has high volume of data.
- All the CPU modules (the maximum number allowed) in the system simultaneously access a module on the extension base unit.

(3) How to reduce processing time

The following methods can be taken for reducing the processing time in a multiple CPU system.

- Mount modules with a large number of access points (such as CC-Link IE, MELSECNET/H, and CC-Link modules) together on the main base unit.
- Set one QCPU as a control CPU for all modules with a large number of access points (such as CC-Link IE, MELSECNET/H, and CC-Link modules) to prevent simultaneous access.
- Reduce the number of refresh points of the CC-Link IE, MELSECNET/H, and CC-Link modules.
- Reduce the number of auto refresh points between CPU modules.

Point

The scan time can be reduced by changing the following PLC parameter settings:(User's Manual (Function Explanation, Program Fundamentals) for the CPU module used)

- "A-PLC Compatibility Setting" (except the Basic model QCPU)
- "Floating Point Arithmetic Processing" (High Performance model QCPU only)

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REVISIONS

*The manual number is given on the bottom left of the back cover.

Print date	Manual number	Revision
January 2004	SH(NA)-080485ENG-A	First edition
May 2005	SH(NA)-080485ENG-B	Partial correction TERMS, Chapter 1, Section 1.1, 2.1, 2.3, 2.4, 3.1, 3.3.1, 3.3.2, 3.4.1, 3.4.2, 3.8, 3.9, 3.10, 4.1.1, 4.1.2, 4.1.3, 6.1, 6.1.1, 7.1, 8.1, 8.2.2, 8.2.3, 8.2.4, 8.3.1, 8.3.4, Appendix 1.1
August 2005	SH(NA)-080485ENG-C	Partial correction TERMS, Section 2.1
April 2007	SH(NA)-080485ENG-D	Universal model QCPU model addition, and revision on the new functions of the Universal model QCPU with a serial number (first five digits) of "09012" Model addition Q02UCPU, Q03UDCPU, Q04UDHCPU, Q06UDHCPU, Q61P, QA65B, QA68B Partial correction SAFETY PRECAUTIONS, MANUALS, TERMS, Section 1.1, 1.2, 1.3, 2.1.1, 2.1.2, 2.1.3, 2.2, 2.3, 2.4, 3.1.1, 3.1.2, 3.1.3, Chapter 4, Section 4.1, 4.1.1, 4.1.2, 4.1.3, 4.1.4, 4.1.5, 4.3.2, 5.1, 5.2, 6.1, 6.1.3, 6.1.4, 6.1.7, 6.1.8, 7.1, 8.1, 8.2.1, 8.2.2
August 2007	SH(NA)-080485ENG-E	Model addition QA6ADP Partial correction TERMS, Section 1.1, 1.2, 1.3, 2.1.1, 2.1.2, 2.1.3, 2.2, 2.3, 3.1, 3.1.2, 3.1.3, 3.3.1, 3.8, 4.1, 4.1.2, 4.2.1, 4.3.1, 8.2.2, Appendix 1.1
March 2008	SH(NA)-080485ENG-F	Universal model QCPU model addition Model addition Q13UDHCPU, Q26UDHCPU Partial correction TERMS, Section 1.1.1, 1.2, 1.3, 2.1.1, 2.1.2, 2.1.3, 2.3, 2.4, 3.1, 3.1.1, 3.1.2, 3.1.3, Chapter 4, Section 4.1.2, 4.1.3, 4.1.4, 4.1.5, 4.2.1, 4.3.1, 4.4, 4.5, 5.1, 5.2, 5.3, 6.1, 6.1.8, 7.1, 8.1, 8.2.1, 8.2.2, 8.3.1, 8.3.2 Addition Section 4.3.3
May 2008	SH(NA)-080485ENG-G	Addition of Universal model QCPU and Process CPU models Model addition Q02PHCPU, Q06PHCPU, Q03UDECPU, Q04UDEHCPU, Q06UDEHCPU, Q13UDEHCPU, Q26UDEHCPU Partial correction A term "MELSECNET/G" has been revised to "CC-Link IE Controller Network" through this manual. TERMS, Chapter 1, Section 1.1, 2.1.1, 2.1.2, 2.1.3, 2.2, 2.3, 2.4, 3.1, 3.8, 4.2, 4.3.1, 4.3.3, 5.1, 5.2, 6.1

Print date	Manual number	Revision
December 2008	SH(NA)-080485ENG-H	Addition of Universal model QCPU and C Controller module models Model addition Q00UCPU, Q01UCPU, Q10UDHCPU, Q20UDHCPU, Q10UDEHCPU, Q20UDEHCPU, Q61P-D Partial correction MANUALS, TERMS, Chapter 1, Section 1.1, 1.3, 2.1.1, 2.1.2, 2.1.3, 2.3, 2.4, 3.1, 3.1.2, 3.1.3, 3.2, 3.3.2, 3.7, 3.9, 4.1.1, 4.1.2, 4.1.3, 4.1.4, 4.1.5, 4.3.1, 4.3.3, 4.5, 5.1, 5.2, 7.1, 8.1, 8.2.2
August 2009	SH(NA)-080485ENG-I	Partial correction INTRODUCTION, MANUAL PAGE ORGANIZATION, TERMS, Section 1.1, 2.1.1, 2.1.2, 2.1.3, 2.2, 2.3, 2.4, 3.1, 3.1.2, 3.1.3, 6.1, 8.1
April 2010	SH(NA)-080485ENG-J	Universal model QCPU model addition, and revision on the new functions of the Universal model QCPU with a serial number (first five digits) of "12012" or later Model addition Q50UDEHCPU, Q100UDEHCPU Partial correction SAFETY PRECAUTIONS, INTRODUCTION, MANUALS, MANUAL PAGE ORGANIZATION, TERMS, Section 1.1, 1.2, 2.3, 2.4, 3.1, 3.3.2, 3.7, 4.1.3, 4.1.4, 4.2.1, 4.3.1, 5.1, 5.2, 5.3
June 2011	SH(NA)-080485ENG-K	Model addition Q35DB Partial correction SAFETY PRECAUTIONS, INTRODUCTION, Section 2.1.1, 2.1.3, 2.2, 2.3, 2.4, 3.4.2, 3.10, 3.11, 4.1.2, 4.1.3, 6.1, 6.1.1, 8.2.1, 8.3.1
October 2011	SH(NA)-080485ENG-L	Revision on the new functions of the Universal model QCPU with a serial number (first five digits) of "13102" or later Model addition QA1S51B Partial correction TERMS, Section 1.3, 2.1.1, 2.1.2, 2.1.3, 2.4, 7.1
May 2012	SH(NA)-080485ENG-M	Motion CPU model addition Model addition Q172DCPU-S1, Q173DCPU-S1, Q172DSCPU, Q173DSCPU Partial correction INTRODUCTION, TERMS, Section 1.1, 1.2, 1.3, 2.1.2, 2.1.3, 2.3, 2.4, 3.1, 3.1.3, 3.8.1, 3.11, Chapter 4, Section 4.1.3, 4.1.4, 4.1.5, 4.2, 4.2.1, 4.3, 4.3.1, 4.4, 4.5, 5.1, 5.2, 6.1.8
November 2012	SH(NA)-080485ENG-N	C Controller model addition Model addition Q24DHCCPU-V Partial correction TERMS, Section 1.1, 1.2, 1.3, 2.1.1, 2.1.2, 2.1.3, 2.3, 3.1, 3.1.1, 3.1.2, 3.1.3, 3.8.1, 3.11, Chapter 4, Section 4.1.3, 4.1.4, 4.1.5, 4.2.1, 4.4, 4.5, 6.1.8
March 2013	SH(NA)-080485ENG-O	Complete revision due to layout change of the manual, and Universal model QCPU model addition Model addition Q03UDVCPU, Q04UDVCPU, Q06UDVCPU, Q13UDVCPU, Q26UDVCPU

Print date	Manual number	Revision
September 2013	SH(NA)-080485ENG-P	C Controller model addition Model addition Q24DHCCPU-LS Partial correction MANUALS, TERMS, Chapter 1, Section 3.1.1, 3.1.2, 3.1.3, 3.2.1, 3.2.2, 3.2.3, 3.3.1, 3.3.2, 3.4, 3.5, 4.2.2, 4.4.1, 4.6, Chapter 6, Section 6.1.1, 6.1.2, 6.1.3, 6.1.4, 6.5, Appendix 2, 3, 4.2
January 2014	SH(NA)-080485ENG-Q	Partial correction Section 3.1.3, 3.5, 4.6
July 2014	SH(NA)-080485ENG-R	Model addition QA1S6ADP Partial correction TERMS, Section 3.2.1, 3.3.1, 3.5, Appendix 2
January 2016	SH(NA)-080485ENG-S	C Controller module model addition Model addition Q26DHCCPU-LS Partial correction TERMS, Section 3.1.1, 3.1.2, 3.2.1, 3.2.2, 3.2.3, 3.3.1, 3.3.2, 4.2.2, 4.4.1, Chapter 6, Section 6.1.2, 6.1.3, 6.1.4, 6.5, Appendix 2
July 2016	SH(NA)-080485ENG-T	C Controller model addition Model addition Q24DHCCPU-VG Partial correction TERMS, Section 3.1.1, 3.1.2, 3.2.1, 3.2.2, 3.2.3, 3.3.1, 3.3.2, 4.2.2, 4.4.1, Chapter 6, Section 6.1.2, 6.1.3, 6.1.4, 6.5, Appendix 2
September 2018	SH(NA)-080485ENG-U	Model addition Q04UDPVCPU, Q06UDPVCPU, Q13UDPVCPU, Q26UDPVCPU Partial correction INTRODUCTION, TERMS, Chapter 1, Section 3.2.1, 3.2.2, 3.2.3, 3.3.1, 3.3.2, 3.4, 3.5, Appendix 2
April 2019	SH(NA)-080485ENG-V	Partial correction TERMS, Section 3.3.1

Japanese manual version SH-080475-V

WARRANTY

Please confirm the following product warranty details before using this product.

1. Gratis Warranty Term and Gratis Warranty Range

If any faults or defects (hereinafter "Failure") found to be the responsibility of Mitsubishi occurs during use of the product within the gratis warranty term, the product shall be repaired at no cost via the sales representative or Mitsubishi Service Company.

However, if repairs are required onsite at domestic or overseas location, expenses to send an engineer will be solely at the customer's discretion. Mitsubishi shall not be held responsible for any re-commissioning, maintenance, or testing on-site that involves replacement of the failed module.

[Gratis Warranty Term]

The gratis warranty term of the product shall be for one year after the date of purchase or delivery to a designated place. Note that after manufacture and shipment from Mitsubishi, the maximum distribution period shall be six (6) months, and the longest gratis warranty term after manufacturing shall be eighteen (18) months. The gratis warranty term of repair parts shall not exceed the gratis warranty term before repairs.

[Gratis Warranty Range]

(1) The range shall be limited to normal use within the usage state, usage methods and usage environment, etc., which follow the conditions and precautions, etc., given in the instruction manual, user's manual and caution labels on the product.

(2) Even within the gratis warranty term, repairs shall be charged for in the following cases.

1. Failure occurring from inappropriate storage or handling, carelessness or negligence by the user. Failure caused by the user's hardware or software design.
2. Failure caused by unapproved modifications, etc., to the product by the user.
3. When the Mitsubishi product is assembled into a user's device, Failure that could have been avoided if functions or structures, judged as necessary in the legal safety measures the user's device is subject to or as necessary by industry standards, had been provided.
4. Failure that could have been avoided if consumable parts (battery, backlight, fuse, etc.) designated in the instruction manual had been correctly serviced or replaced.
5. Failure caused by external irresistible forces such as fires or abnormal voltages, and Failure caused by force majeure such as earthquakes, lightning, wind and water damage.
6. Failure caused by reasons unpredictable by scientific technology standards at time of shipment from Mitsubishi.
7. Any other failure found not to be the responsibility of Mitsubishi or that admitted not to be so by the user.

2. Onerous repair term after discontinuation of production

(1) Mitsubishi shall accept onerous product repairs for seven (7) years after production of the product is discontinued. Discontinuation of production shall be notified with Mitsubishi Technical Bulletins, etc.

(2) Product supply (including repair parts) is not available after production is discontinued.

3. Overseas service

Overseas, repairs shall be accepted by Mitsubishi's local overseas FA Center. Note that the repair conditions at each FA Center may differ.

4. Exclusion of loss in opportunity and secondary loss from warranty liability

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(1) Damages caused by any cause found not to be the responsibility of Mitsubishi.

(2) Loss in opportunity, lost profits incurred to the user by Failures of Mitsubishi products.

(3) Special damages and secondary damages whether foreseeable or not, compensation for accidents, and compensation for damages to products other than Mitsubishi products.

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SH(NA)-080485ENG-V(1904)MEE
MODEL: QCPU-U-MA-E
MODEL CODE: 13JR75

MITSUBISHI ELECTRIC CORPORATION

HEAD OFFICE : TOKYO BUILDING, 2-7-3 MARUNOUCHI, CHIYODA-KU, TOKYO 100-8310, JAPAN
NAGOYA WORKS : 1-14 , YADA-MINAMI 5-CHOME , HIGASHI-KU, NAGOYA , JAPAN