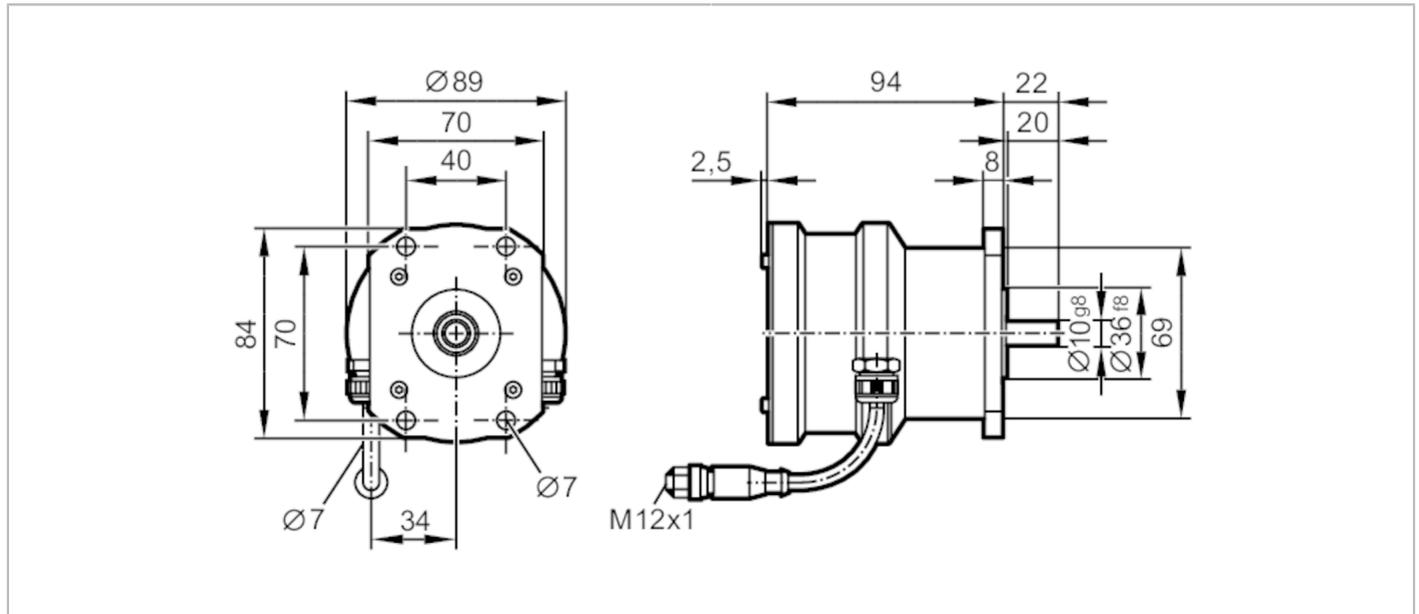


RN6066



Absoluter Singleturn-Einzeldrehgeber mit Vollwelle

RN-8192-S24/S



Product characteristics	
Resolution	8192 revolutions; 13 bit
Communication interface	SSI data interface
Shaft design	solid shaft
Shaft diameter [mm]	10
Application	
Function principle	absolute
Revolution type	singleturn
Electrical data	
Operating voltage [V]	10...30 DC
Current consumption [mA]	< 100
Inputs	
Inputs	reversal of direction of rotation; reset to zero
Outputs	
Code	Gray code; (increasing code values when turned clockwise (seen on the shaft))
Code signal	Clock input; TTL-compatible signals; clock and clock (inv.) from drivers to RS 422; data output; synchronous serial; TTL-compatible signal data and data (inv.)
Measuring/setting range	
Resolution	8192 revolutions; 13 bit
Interfaces	
Communication interface	SSI data interface
Operating conditions	
Ambient temperature [°C]	-40...100
Max. relative air humidity [%]	98
Protection	IP 67

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Tests / approvals		
Shock resistance	EN 60068-2-27	< 50 g 6 ms
Vibration resistance	EN 60068-2-6	< 10 g / 55...2000 Hz
MTTF [years]	289	
Mechanical data		
Weight [g]	1113.3	
Dimensions [mm]	Ø 89 / L = 116	
Material	flange: aluminum anodized ; housing: aluminum anodized	
Max. revolution, mechanical [U/min]	6000	
Max. starting torque [Nm]	4	
Reference temperature torque [°C]	25	
Shaft design	solid shaft	
Shaft diameter [mm]	10	
Shaft material	stainless steel (1.4305 / 303)	
Max. shaft load axial (at the shaft end) [N]	40	
Max. shaft load radial (at the shaft end) [N]	110	
Remarks		
Remarks	Wires/pins not connected (n.c.) must not be used.	
Electrical connection		
Cable: 0.15 m, PUR		
Connection		
Connector: 1 x M12		
1	reversal of direction of rotation ccw = permanently active HIGH signal when the shaft stands still	
2	reset to zero connect pins 8 and 2 for 30 seconds for a reset to 0	
3	data activated: HIGH > 0.7 x L+ disabled: LOW < 0.3 x L+	
4	data (inv.)	
5	0 V	
6	clock (inv.)	
7	clock Monoflop startet mit negativer Flanke	
8	L + screen housing	

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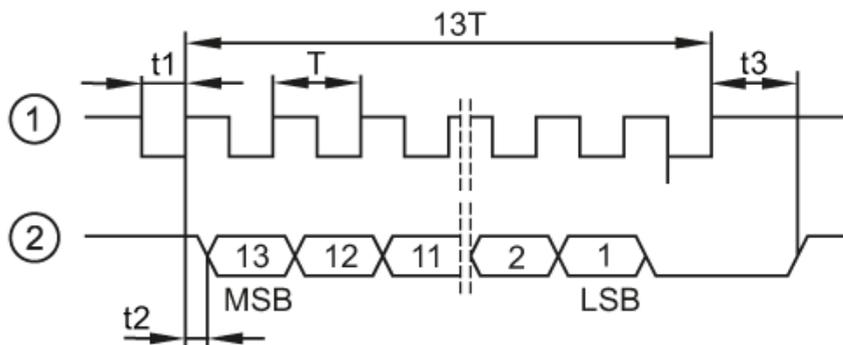


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RN-8192-S24/S

Other data

Diagrams and graphs



1 clock

2 data

$t1 \leq 0.5 \mu\text{s}$ clock: 1 MHz

$t2 < 0.4 \mu\text{s}$

$t3 = 13 \dots 20 \mu\text{s}$

$T = 1 \dots 10 \mu\text{s}$

13 Bit without parity bit